SEMINAR

On

INTEL FPGA Based Hardware Implementation

13th February, 2017

Organized by:

Department of Electronics
&
Instrumentation Engineering

In collaboration with

Enixs Technology India Pvt Ltd

Guru Nanak Institute of Technology
157/F, Nilgunj Road, Sodepur
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7. Mrs. Saswati Chatterjee
8. Mrs Nabamita Paul
9. Mr. Mrinmoy Dutta

Program Schedule

Registration	: 1:00 pm
Technical Session I	: 1:30 p.m. - 3:00 p.m.
Technical Session II	: 3:15 p.m. – 5:00 p.m.
Valedictory Session	: 5.15 p.m.

Participants

- Faculty Members
- Technical Staff
- Students

Mode of Selection

The filled registration form with self-signature is to be submitted to Registration committee members by 10.02.2017. Registration forms are available from the department. Application will be accepted on a first come first serve basis.

No Registration Fee

Venue and Time

The Seminar will be held in Seminar Hall, GNIT, Panihati, Sodepur, Kol-114 from 1:00 p.m. to 5:30p.m.

Contact Person

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