Paper Name: ANALOG ELECTRONIC CIRCUITS

Paper Code: EC 402

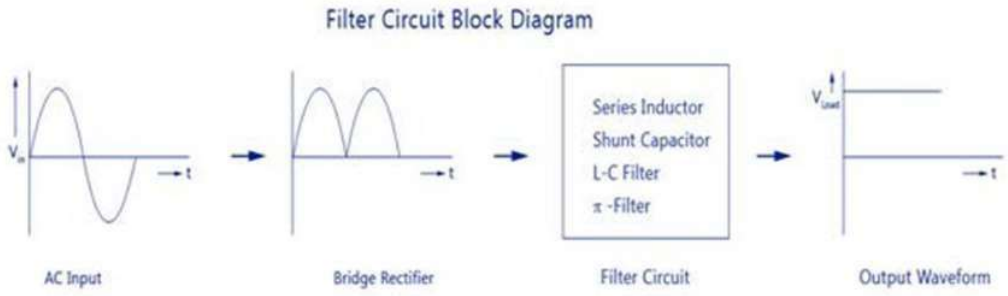
Contacts : 3L

Credits :3

Prepared by: Ms.Soma Boral, Dr. Nabaneeta Banerjee

Module I: Filters & Regulators:

Passive filters:



We have learnt in rectifier circuits about converting a sinusoidal ac voltage into its corresponding pulsating dc. Apart from the dc component, this pulsating dc voltage will have unwanted ac components like the components of its supply frequency along with its harmonics (together called ripples). These ripples will be the highest for a single-phase half wave rectifier and will reduce further for a single-phase full wave rectifier. The ripples will be minimum for 3-phase rectifier circuits. Such supply is not useful for driving complex electronic circuits. For most supply purposes constant dc voltage is required than the pulsating output of the rectifier. For most applications the supply from a rectifier will make the operation of the circuit poor. If the rectifier output is smoothened and steady and then passed on as the supply voltage, then the overall operation of the circuit becomes better. Thus, the output of the rectifier has to be passed though a filter circuit to filter the ac components.

The filter is a device that allows passing the dc component of the load and blocks the ac component of the rectifier output. Thus the output of the filter circuit will be a steady dc voltage.

The filter circuit can be constructed by the combination of components like capacitors, resistors, and inductors. Inductor is used for its property that it allows only dc components to pass and blocks ac signals. Capacitor is used so as to block the dc and allows ac to pass. All the combinations and their working are explained in detail below.

Series Inductor Filter:

The circuit diagram of a full wave rectifier with a series inductor filter is given below.

As the name of the filter circuit suggests, the Inductor L is connected in series between the rectifier circuit and the load. The inductor carries the property of opposing the change in current that flows through it.

In other words, the inductor offers high impedance to the ripples and no impedance to the desired dc components. Thus the ripple components will be eliminated. When the rectifier output current increases above a certain value, energy is stored in it in the form of a magnetic field and this energy is given up when the output current falls below the average value. Thus all the sudden changes in current that occurs in the circuit will be smoothened by placing the inductor in series between the rectifier and the load.

The waveform below shows the use of inductor in the circuit.

From the circuit, for zero frequency dc voltage, the choke resistance Ri in series with the load resistance RL forms a voltage divider circuit, and thus the dc voltage across the load is

$$V_{dc} = R_L/(R_i + R_L)$$

Vdc is the output from a full wave rectifier. In this case, the value of Ri is negligibly small when compared to RL.

The effect of higher harmonic voltages can be easily neglected as better filtering for the higher harmonic components take place. This is because of the fact that with the increase in frequency, the reactance of the inductor also increases. It should be noted that a decrease in the value of load resistance or an increase in the value of load current will decrease the amount of ripples in the circuit. So, the series inductor filter is mostly used in cases of high load current or small load resistance. A simple series inductor filter may not be properly used. It is always better to use a shunt capacitor (C) with series inductor (L) to form an LC Filter.

Shunt Capacitor Filter:

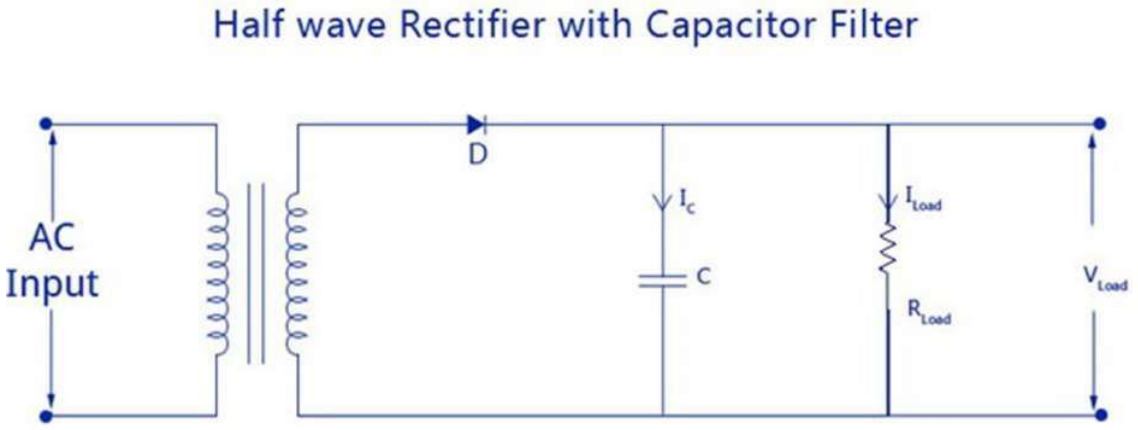
As the name suggests, a capacitor is used as the filter and this high value capacitor is shunted or placed across the load impedance. This capacitor, when placed across a rectifier gets charged and stores the charged energy during the conduction period. When the rectifier is not conducting, this energy charged by the capacitor is delivered back to the load. Through this energy storage and delivery process, the time duration during which the current flows through the load resistor gets increased and the ripples are decreased by a great amount. Thus for the ripple component with a frequency of ‘f’ megahertz, the capacitor ‘C’ will offer a very low impedance. The value of this impedance can be written as:

Shunt Capacitor Impedance = 1/2 fC

Thus the dc components of the input signal along with the few residual ripple components, is only allowed to go through the load resistance RLoad. The high amount of ripple components of current gets bypassed through the capacitor C.

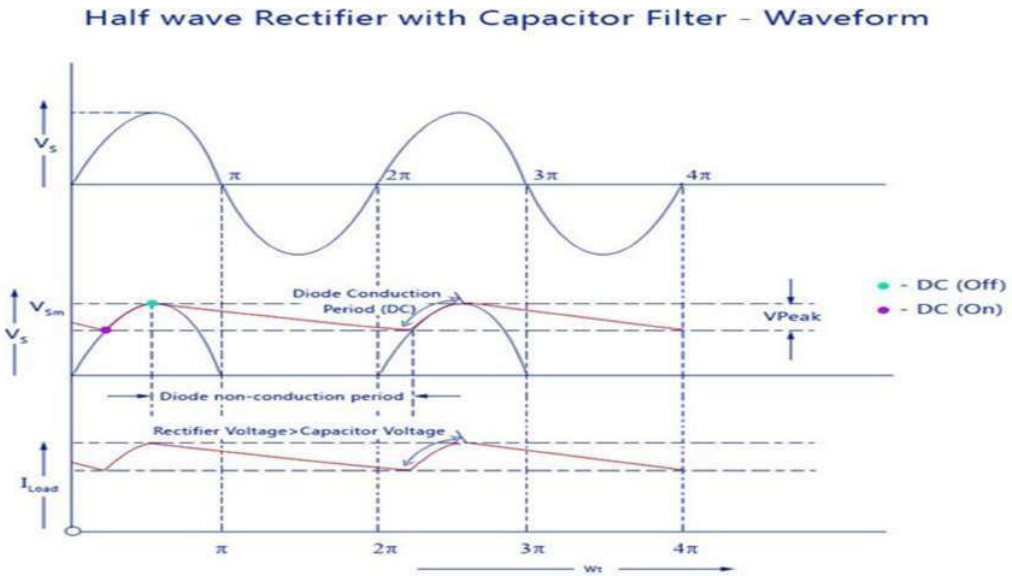
Now let us look at the working of Half-wave rectifier and Full-wave rectifier with Capacitor filters, their output filtered waveform, ripple factor, merits and demerits in detail.

2.1 Half-wave Rectifier with Capacitor Filter



The circuit diagram above shows a half-wave rectifier with a capacitor filter. The filter is applied across the load RLoad. The output of the RLoad is VLoad, the current through it is ILoad. The current through the capacitor is Ic.

During the positive half cycle of the input ac voltage, the diode D will be forward biased and thus starts conducting. During this period, the capacitor 'C' starts charging to the maximum value of the supply voltage Vsm. When the capacitor is fully charged, it holds the charge until the input ac supply to the rectifier reaches the negative half cycle. As soon as the negative half supply is reached, the diode gets reverse biased and thus stops conducting. During the non-conducting period, the capacitor 'C' discharges all the stored charges through the output load resistance RLoad. As the voltage across RLoad and the voltage across the capacitor 'C' are the same (VLoad = Vc), they decrease exponentially with a time constant (C*RLoad) along the curve of the non-conducting period. This is shown in the graph below.



The value of the discharge time constant (C*RLoad) being very large, the capacitor ‘C’ will not have enough time to discharge properly. As soon as the capacitor starts discharging, the time becomes over. Thus the value of RLoad at the discharge time will also be high and have just a little less value that the output of RLoad. This is when the positive half cycle repeats again and the diode starts conducting. The condition to be considered at this stage is that the rectified voltage takes value more than the capacitor voltage . When the condition occurs the capacitor starts charging to a value of Vsm. The condition again changes when the negative half cycle comes into pace, and the whole cycle is again repeated to form the output waveform as shown above. The output shows a nearly constant dc voltage at the load and that the output voltage is increased considerably.

Thus, in short:

- If the value of load resistance is large, the discharge time constant will be of a high value, and thus the capacitors’ time to discharge will get over soon. This lowers the amount of ripples in the output and increases the output voltage. If the load resistance is small, the discharge time constant will be less, and the ripples will be more with decrease in output voltage.
- The value of the capacitor used plays an important role in determining the output ripples and the average dc level. If the capacitor value is high, the amount of charge it can store will be high and the amount it discharges will be less. Thus the ripples will be less and the average dc level will be high. But, there is a limit on how much capacitance can b increased. If the capacitor value is increased to a very high value, the amount of current required to charge the capacitor to a given voltage will be high. This value of current depends on the manufacturer of the diode and will be surely limited to a

certain value. Thus, there is a limit in increasing the capacitor value in a half-wave rectifier shunt capacitor filter circuit.

- Poor voltage regulation.

Ripple Factor

The rms value depends on the peak value of charging and discharging magnitude, Vpeak.

Vac rms = Vpeak/2

Vpeak = Idc/fC

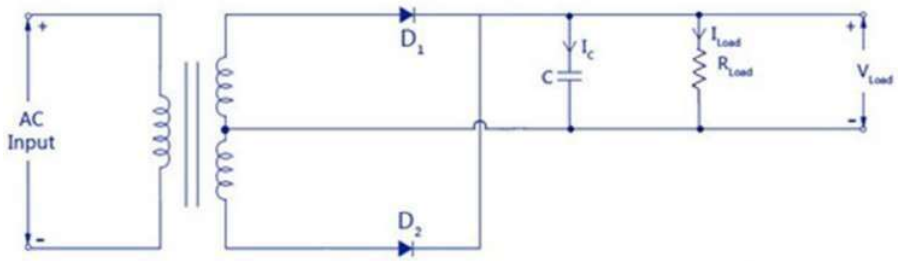
Ripple Factor = Vac rms/Vdc = (Vpeak/2) * (1/Idc.RLoad)

= Idc/(2 .Idc.RLoad.f.C) = 1/(2 fCRLoad)

2.2 Full-wave Rectifier with Shunt Capacitor Filter

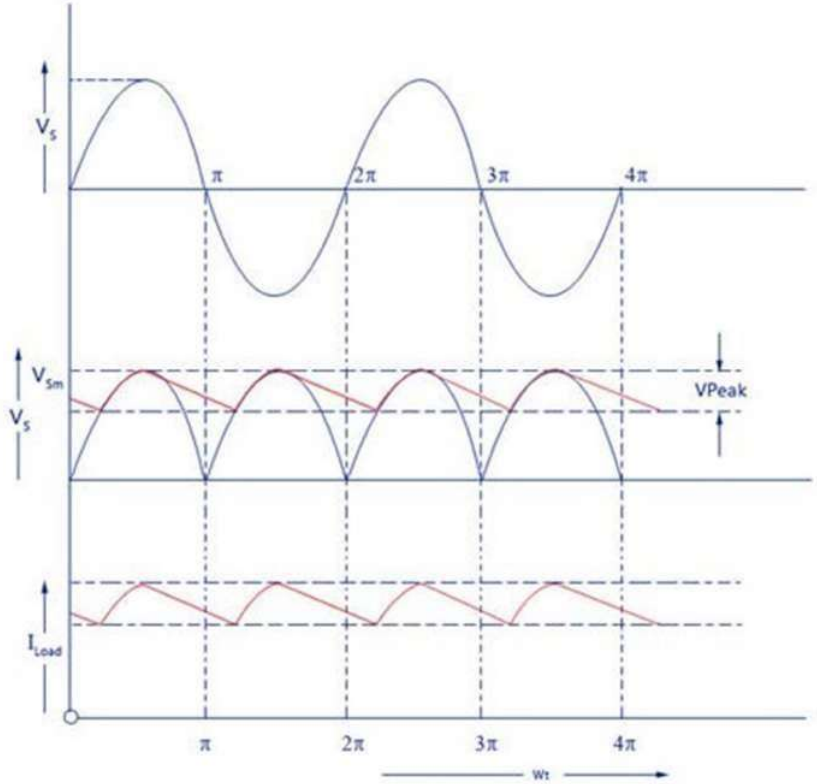
The circuit diagram of a full-wave rectifier wit capacitor filter is shown below.

Fullwave Rectifier with Capacitor Filter



The filter capacitor C is placed across the resistance load RLoad. The whole working is pretty much similar to that of a half-wave rectifier with shunt capacitor explained above. The only difference is that two pulses of current will charge the capacitor during alternate positive (D1) and negative (D2) half cycles. Similarly capacitor C discharges twice through RLoad during one full cycle. This is shown in the waveform below.

Fullwave Rectifier with Capacitor Filter - Waveform



The load current reduces by a smaller amount before the next pulse is received as there are 2 current pulses per cycle. This causes a good reduction in ripples and a further increase in the average dc load current.

L-C Filters:

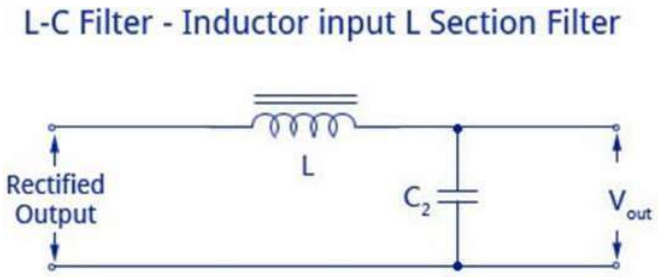
In the simple shunt capacitor filter circuit explained above, we have concluded that the capacitor will reduce the ripple voltage, but causes the diode current to increase .This large current may damage the diode and will further cause heating problem and decrease the efficiency of the filter. On the other hand, a simple series inductor reduces both the peak and effective values of the output current and output voltage. Then if we combine both the filter (L and C), a new filter called the L-C filter can be designed which will have a good efficiency, with restricted diode current and enough ripple removal factor .The voltage stabilizing action of shunt capacitor and the current smoothing action of series inductor filter can be combined to form a perfect practical filter circuit.

L-C filters can be of two types: Choke Input L-section Filter and L-C Capacitor input filter

Choke Input L-Section Filter:

An inductor filter increases the ripple factor with the increase in load current Rload. A capacitor filter has an inversely proportional ripple factor with respect to load resistance. Economically, both inductor filter and capacitor filter are not suitable for high end purpose

L-C inductor input or L-section filter consists of an inductor ' L' connected in series with a half or full wave rectifier and a capacitor 'C' across the load. This arrangement is also called a choke input filter or L-section filter because it's shape resembles and inverted L-shape. To increase the smoothing action using the filter circuit, just one L-C circuit will not be enough. Several L-section filters will be arranged to obtain a smooth filtered output. The circuit diagram and smoothened waveform of a Full wave rectifier output is shown below.



As shown in the circuit diagram above, the inductor L allows the dc to pass but restricts the flow of ac components as its dc resistance is very small and ac impedance is large. After a signal passes through the choke, if there is any fluctuation remaining the current, it will be fully bypassed before it reaches the load by the shunt capacitor because the value of Xc is much smaller than Rload. The number of ripples can be reduced to a great amount by making the value of XL greater than Xc at ripple frequency.

Ripple Factor:

Ripple Factor = Vac rms/Vdc = $(\sqrt{2}/3)(Xc/XL) = (\sqrt{2}/3)(1/[2wc])(1/[2wL]) = 1/(6\sqrt{2}w^2LC)$

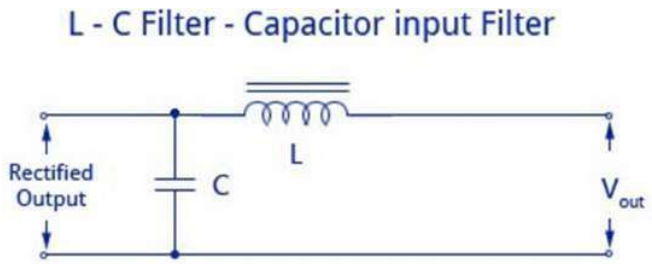
Though the L-C filter has all these advantages, it has now become quite obsolete due the huge size of inductors and its cost of manufacturing. Nowadays, IC voltage regulators are more commonly used along with active filters, that reduce the ripples and keeps the output dc voltage constant.

The diagram of L-C Capacitor input filter and waveform is shown below.

Π – Filter or Capacitance Input Filter:

The name pi – Filter implies to the resemblance of the circuit to a Π shape with two shunt capacitances (C1 and C2) and an inductance filter 'L'. As the rectifier output is provided directly into the capacitor it also called a capacitor input filter.

The output from the rectifier is first given to the shunt capacitor C. The rectifier used can be half or full wave and the capacitors are usually electrolytic even though they large in size. In practical applications, the two capacitances are enclosed in a metal container which acts as a common ground for the two capacitors. Circuit diagram and the waveform are given below.



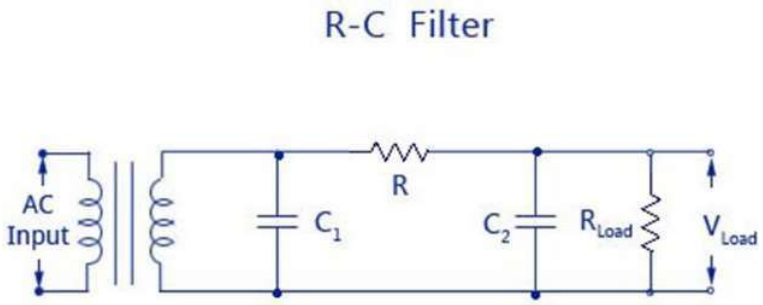
When compared to other type of filters, the Π – Filter has some advantages like higher dc voltage and smaller ripple factor. But it also has some disadvantages like poor voltage regulation, high peak diode current, and high peak inverse voltage.

This filter is divided into two – a capacitor filter and a L-section filter. The capacitor C1 does most of the filtering in the circuit and the remaining ripple os removed by the L-section filter (L-C2). C1 is selected to provide very low reactance to the ripple frequency. The voltage regulation is poor for this circuit as the output voltage falls off rapidly with the increase in load current.

Ripple Factor:

Ripple Factor = $\sqrt{2}/(8w^3C1C2LRload)$ R-C Filter:

We have already discussed about the drawbacks of using a pi-filter. The main reason for all these drawbacks is the use of inductor in the filter circuit. If we use a resistance in series, instead of the inductor as the filter, these drawbacks can be overcome. Thus the circuit is named as R-C filter. In this circuit, the ripples have to be made to drop across the resistance R instead of the load resistance RL. For this, the value of RL is kept much larger than the value of reactance of capacitor C2 (XC2). This means that each section reduces the ripple by a factor of at least 10.

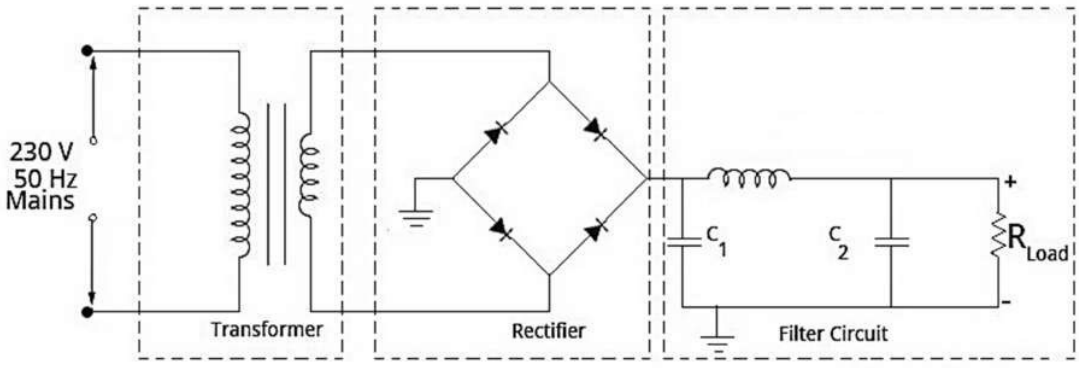


Though the circuit nullifies certain drawbacks of the pi-filter, the circuit on its own has some problems as well. The filter has very poor voltage regulation. There is a large voltage drop in the resistance R. The circuit also develops a lot of heat and this has to be dissipated through enough and adequate ventilation.

Thus, the filter is only suitable for small load current or large load resistance circuits.

INTRODUCTION:

Almost all basic household electronic circuits need an unregulated AC to be converted to constant DC, in order to operate the electronic device. All devices will have a certain power supply limit and the electronic circuits inside these devices must be able to supply a constant DC voltage within this limit. That is, all the active and passive electronic devices will have a certain DC operating point (Q-point or Quiescent point), and this point must be achieved by the source of DC power. The DC power supply is practically converted to each and every stage in an electronic system. Thus a common requirement for all this phases will be the DC power supply. All low power system can be run with a battery. But, for long time operating devices, batteries could prove to be costly and complicated. The best method used is in the form of an unregulated power supply –a combination of a transformer, rectifier and a filter. The diagram is shown below.



Unregulated Power Supply – Diagram

As shown in the figure above, a small step down transformer is used to reduce the voltage level to the devices needs. In India, a 1 Ø supply is available at 230 volts. The output of the transformer is a pulsating sinusoidal AC voltage, which is converted to pulsating DC with the help of a rectifier. This output is given to a filter circuit which reduces the AC ripples, and passes the DC components. But here are certain disadvantages in using an unregulated power supply.

1. Poor Regulation – When the load varies, the output does not appear constant. The output voltage changes by a great value due to the huge change in current drawn from the supply. This is mainly due to the high internal resistance of the power supply (>30 Ohms).

2. AC Supply Main Variations – The maximum variations in AC supply mains is give or take 6% of its rated value . But this value may go higher in some countries (180-280 volts). When the value is higher it's DC voltage output will differ largely.
3. Temperature Variation – The use of semiconductor devices in electronic devices may cause variation in temperature.

These variations in dc output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. For instance, in oscillators the frequency will shift, in transmitters output will get distorted, and in amplifiers the operating point will shift causing bias instability.

All the above listed problems are overcome with the help of a voltage regulator which is employed in conjunction with an unregulated power supply. Thus, the ripple voltage is largely reduced. Thus, the supply becomes a regulated power supply.

The internal circuitry of a regulated power supply also contains certain current limiting circuits which helps the supply circuit from getting fried from inadvertent circuits. Nowadays, all the power supplies use IC's to reduce ripples, enhance voltage regulation and for widened control options. Programmable power supplies are also available to allow remote operation that is useful in many settings.

Voltage regulator circuit:

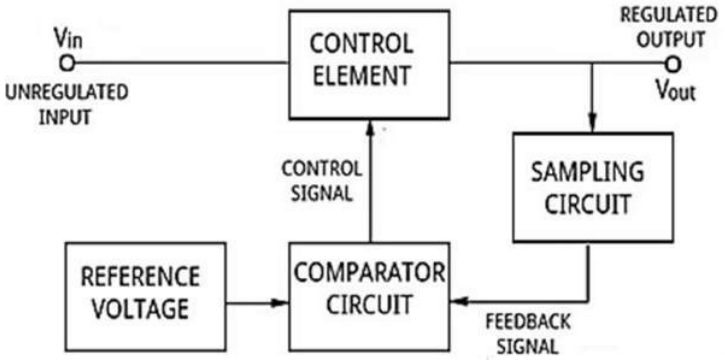
A voltage regulator is a voltage stabilizer that is designed to automatically stabilize a constant voltage level. A voltage regulator circuit is also used to change or stabilize the voltage level according to the necessity of the circuit. Thus, a voltage regulator is used for two reasons:-

1. To regulate or vary the output voltage of the circuit.
2. To keep the output voltage constant at the desired value in-spite of variations in the supply voltage or in the load current.

All electronic voltage regulators will have a stable voltage reference source which is provided by the reverse breakdown voltage operating diode called zener diode. The main reason to use a voltage regulator is to maintain a constant dc output voltage. It also blocks the ac ripple voltage that cannot be blocked by the filter.

Discrete Transistor Series Voltage Regulator:

The block diagram of a discrete transistor type voltage regulator is given below. A control element is placed to collect the unregulated input which controls the magnitude of the input voltage and passes it to the output. The output voltage is then feedback to a sampling circuit and then compared with a reference voltage and sent back to the output.

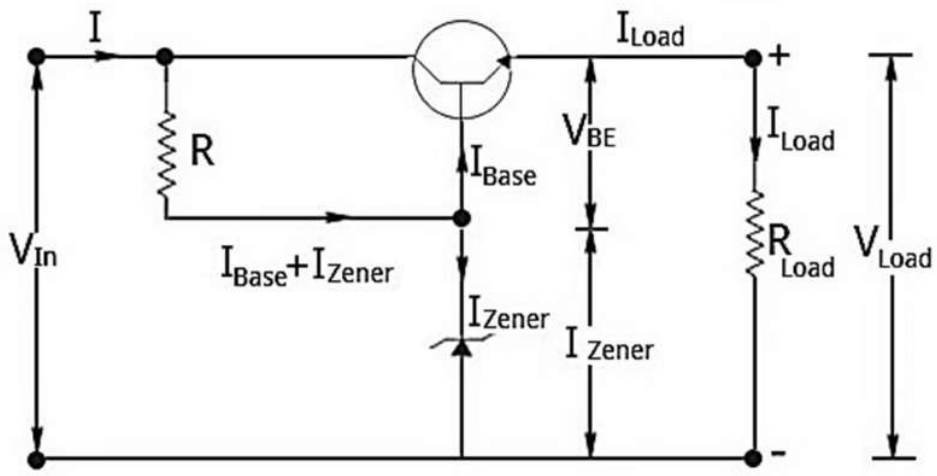


Block Diagram of Series Voltage Regulator

Thus, if the output voltage tends to increase the comparator circuit provides a control signal to cause the control element to reduce the magnitude of the output voltage by passing it through the sampling circuit and comparing it, thereby maintaining a constant and steady output voltage.

Suppose the output voltage tends to decrease, the comparator circuit provides a control signal that causes the series control element to increase the magnitude of output voltage, thus maintaining the steadiness.

Circuit diagram of series voltage regulator:



Such a circuit is also named an emitter follower voltage regulator. It is called so because the transistor used is connected in an emitter follower configuration. The circuit consists of an N-P-N transistor and a

zener diode. As shown in the figure below, the collector and emitter terminals of the transistor are in series with the load. Thus this regulator has the name series in it. The transistor used is a series pass transistor.

The output of the rectifier that is filtered is then given to the input terminals and regulated output voltage Vload is obtained across the load resistor Rload. The reference voltage is provided by the zener diode and the transistor acts as a variable resistor, whose resistance varies with the operating conditions of base current, Ibase.

The main principle behind the working of such a regulator is that a large proportion of the change in supply or input voltage appears across the transistor and thus the utput voltage tends to remain constant.

The output voltage can thus be written as

Vout = Vzener – Vbe

The transistor base voltage Vbase and the zener diode voltage Vzener are equal and thus the value of Vbase remains almost constant.

Operation

When the input supply voltage Vin increases the output voltage Vload also increases. This increase in Vload will cause a reduced voltage of the transistor base emitter voltage Vbe as the zener voltage Vzener is constant. This reduction in Vbe causes a decrease in the level of conduction which will further increase the collector-emitter resistance of the transistor and thus causing an increase in the transistor collector- emitter voltage and all of this causes the output voltage Vout to reduce. Thus, the output voltage remains constant. The operation is similar when the input supply voltage decreases.

The next condition would be the effect of the output load change in regard to the output voltage. Let us consider a case where the current is increased by the decrease in load resistance Rload. This causes a decrease in the value of output voltage and thus causes the transistor base emitter voltage to increase. This causes the collector emitter resistance value to decrease due to an increase in the conduction level of the transistor. This causes the input current to increase slightly and thus compensates for the decrease in the load resistance Rload.

The biggest advantage of this circuit is that the changes in the zener current are reduced by a factor β and thus the zener effect is greatly reduced and a much more stabilized output is obtained.

Limitations

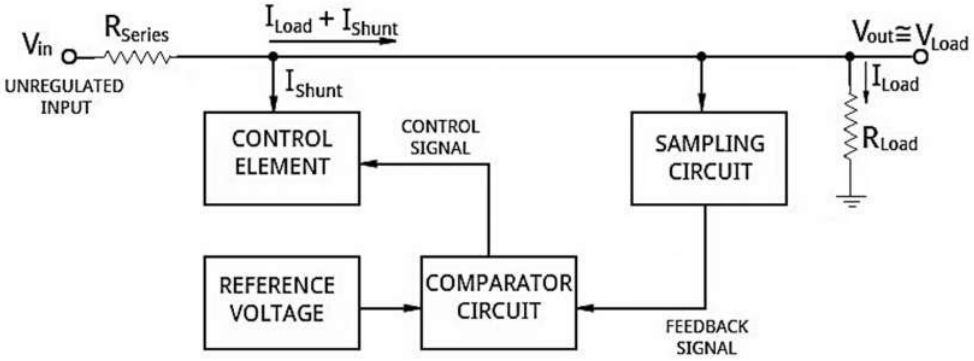
The limitations listed below has proved the use of this series voltage regulator only suitable for low output voltages.

1. With the increase in room temperature, the values of Vbe and Vzener tend to decrease. Thus the output voltage cannot be maintained a constant. This will further increase the transistor base emitter voltage and thus the load.
2. There is no option to change the output voltage in the circuit.
3. Due to the small amplification process provided by only one transistor, the circuit cannot provide good regulation at high currents.

4. When compared to other regulators, this regulator has poor regulation and ripple suppression with respect to input variations.
5. The power dissipation of a pass transistor is large because it is equal to VccIc and almost all variation appears at Vce and the load current is approximately equal to collector current. Thus for heavy load currents pass transistor has to dissipate a lot of power and, therefore, becoming hot.

Discrete Transistor Shunt Voltage Regulator:

The block diagram of a discrete transistor shunt voltage regulator is given below. As the name says the voltage regulation is provided by shunting the current away from the load. The control element shunts a part of the current that is produced as a result of the input unregulated voltage that is given to the load. Thus the voltage is regulated across the load. Due to the change in load, if there is a change in the output voltage, it will be corrected by giving a feedback signal to the comparator circuit which compares with a reference voltage and gives the output control signal to the control element to correct the magnitude of the signal required to shunt the current away from the load.

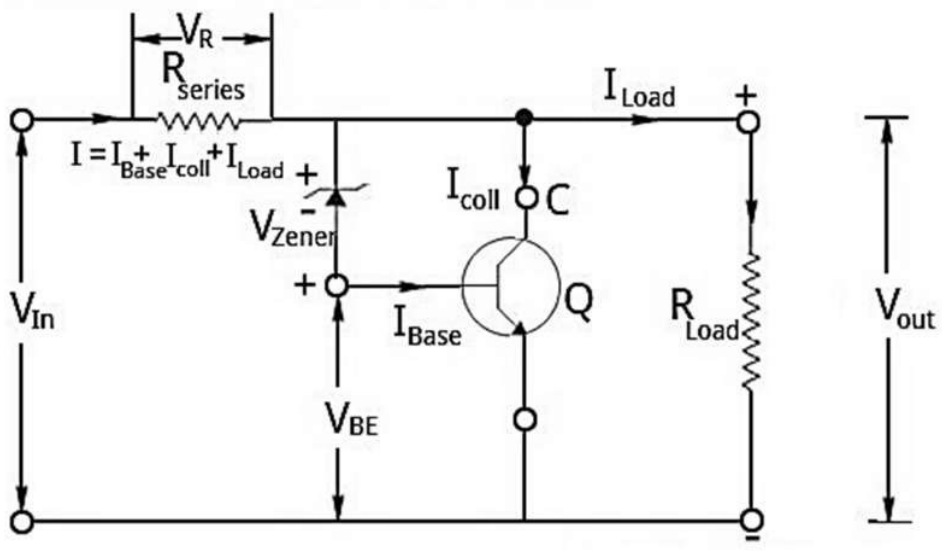


Discrete Transistor Shunt Voltage Regulator

If the output voltage increases, the shunt current increases and thus produces less load current and maintains a regulated output voltage. If the output voltage reduces, the shunt current reduces and thus produces more load current and maintains a regulated constant output voltage. In both cases, the sampling circuit, comparator circuit and control element plays an important role.

Circuit diagram of shunt voltage regulator:

The image below shows the circuit diagram of a shunt voltage regulator. The circuit consists of an NPN transistor and a zener diode along with a series resistor Rseries that is connected in series with the input supply. The zener diode is connected across the base and the collector of the transistor which is connected across the output.



Zener Controlled Transistor Shunt Voltage Regulator

Operation

As there is a voltage drop in the series resistance Rseries the unregulated voltage is also decreased along with it. The amount of voltage drop depends on the current supplied t the load Rload. The value of the voltage across the load depends on the zener diode and the transistor base emitter voltage Vbe.

Thus, the output voltage can be written as

Vout = Vzener + Vbe = Vin – I.Rseries

The output remains nearly a constant as the values of Vzener and Vbe are nearly constant. This condition is explained below.

When the supply voltage increases, the output voltage and base emitter voltage of transistor increases and thus increases the base current Ibase and therefore causes an increase in the collector current Icoll (Icoll = β.Ibase).

Thus, the supply voltage increases causing an increase in supply current, which inturn causes a voltage drop i the series resistance Rseries and thereby decreasing the output voltage. This decrease will be more than

enough to compensate for the initial increase in output voltage. Thus, the output remains nearly a constant. The working explained above happens in reverse if the supply voltage decreases.
When the load resistance Rload decreases, the load current Iload increases due to the decrease in currents through base and collector Ibase and Icoll. Thus, there will not be any voltage drop across Rseries and the input current remains constant. Thus, the output voltage will remain constant and will be the difference of the supply voltage and the voltage drop in the series resistance. It happens in reverse if there is an increase in load resistance.

Limitations

The series resistor causes a huge amount of power loss.

1. The supply current flow will be more through the transistor than it is to be through the load.

2. The circuit may have problems regarding over voltage mishaps.

I.C Voltage regulators:

An IC based voltage regulator can be classified in different ways. A common type of classification is 3 terminal voltage regulator and 5 or multi terminal voltage regulator. Another popular way of classifying IC voltage regulators is by identifying them as linear voltage regulator & switching voltage regulator. There is a third set of classification as 1) Fixed voltage regulators (positive & negative) 2) Adjustable voltage regulators (positive & negative) and finally 3) Switching regulators. In the third classification, fixed & adjustable regulators are basically versions of linear voltage regulators.

Fixed Voltage Regulators:

These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage. All those IC's in the 78XX series are fixed positive voltage regulators. In the IC nomenclature – 78XX ; the part XX denotes the regulated output voltage the IC is designed for. Examples:- 7805, 7806, 7809 etc.

A negative fixed voltage regulator is same as the positive fixed voltage regulator in design, construction & operation. The only difference is in the polarity of output voltages. These IC's are designed to provide a negative output voltage. Example:- 7905, 7906 and all those IC's in the 79XX series.

Power Supply Characteristics:

The quality of the power supply is determined by various characteristics like load voltage, load current, voltage regulation, source regulation, output impedance, ripple rejection, and so on. Some of the characteristics are briefly explained below:

1. Load Regulation – The load regulation or load effect is the change in regulated output voltage when the load current changes from minimum to maximum value.

Load regulation = Vno-load – Vfull-load

Vno-load – Load Voltage at no load

Vfull-load – Load voltage at full load.
From the above equation we can understand that when Vno-load occurs the load resistance is infinite, that is, the out terminals are open circuited. Vfull-load occurs when the load resistance is of the minimum value where voltage regulation is lost.

% Load Regulation = [(Vno-load – Vfull-load)/Vfull-load] * 100

2. Minimum Load Resistance – The load resistance at which a power supply delivers its full-load rated current at rated voltage is referred to as minimum load resistance.

Minimum Load Resistance = Vfull-load/Ifull-load

The value of Ifull-load, full load current should never increase than that mentioned in the data sheet of the power supply.

3. Source/Line Regulation – In the block diagram, the input line voltage has a nominal value of 230 Volts but in practice, there are considerable variations in ac supply mains voltage. Since this ac supply mains voltage is the input to the ordinary power supply, the filtered output of the bridge rectifier is almost directly proportional to the ac mains voltage.

The source regulation is defined as the change in regulated output voltage for a specified rage of line voltage.

4. Output Impedance – A regulated power supply is a very stiff dc voltage source. This means that the output resistance is very small. Even though the external load resistance is varied, almost no change is seen in the load voltage. An ideal voltage source has an output impedance of zero.

5. Ripple Rejection – Voltage regulators stabilize the output voltage against variations in input voltage. Ripple is equivalent to a periodic variation in the input voltage. Thus, a voltage regulator attenuates the ripple that comes in with the unregulated input voltage. Since a voltage regulator uses negative feedback, the distortion is reduced by the same factor as the gain.

SMPS:

Switch mode power supplies (SMPSs) are used in a range of applications as an efficient and effective source of power. This is in major part to their efficiency. For anybody still working on a desktop, look for the fan output in the central processing units (CPU). That's where the SMPS is. SMPS offers advantages in terms of size, weight, cost, efficiency and overall performance. These have become an accepted part of electronics gadgets. Basically it is a device in which energy conversion and regulation is provided by power semiconductors that are continuously switching "on" and "off" with high frequency.

The different kinds

- D.C. to D.C. Converter Forward Converter:

- Flyback Converter:
- Self-Oscillating Flyback Converter

DC-DC converter:

The primary power received from AC main is rectified and filtered as high voltage DC. It is then switched at a huge rate of speed and fed to the primary side of the step-down transformer. The step-down transformer is only a fraction of the size of a comparable 50 Hz unit thus relieving the size and weight problems. We have the filtered and rectified output at the secondary side of the transformer. It is now sent to the output of the power supply. A sample of this output is sent back to the switch to control the output voltage.

Forward converter:

In a forward converter the choke carries the current when the transistor is conducting as well as when it's not. The diode carries the current during the OFF period of the transistor. Therefore, energy flows into the load during both the periods. The choke stores energy during the ON period and also passes some energy into the output load.

Flyback converter:

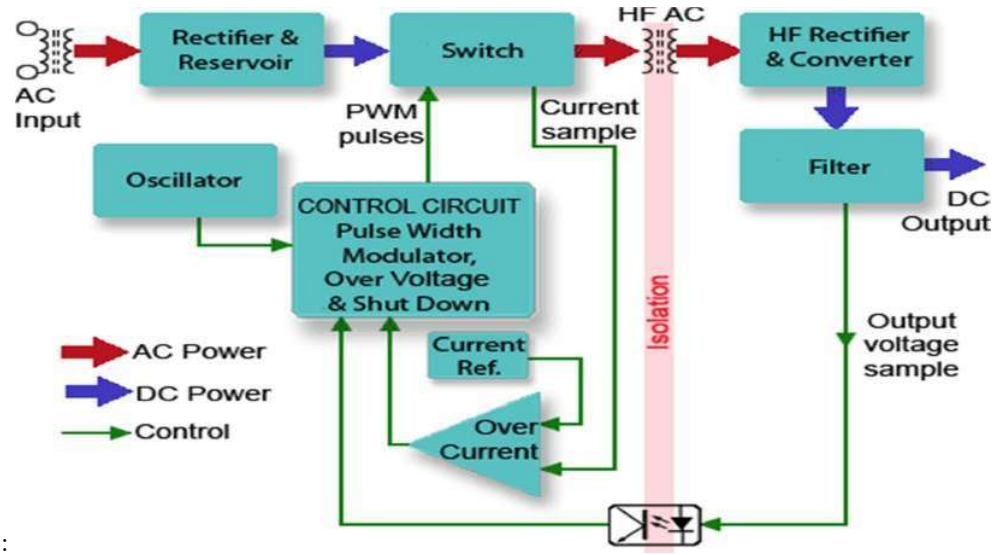
In a flyback converter, the magnetic field of the inductor stores energy during the ON period of the switch. The energy is emptied into the output voltage circuit when the switch is in the open state. The duty cycle determines the output voltage.

Self-Oscillating Flyback Converter:

This is the most simple and basic converter based on the flyback principle.During the conduction time of the switching transistor, the current through the transformer primary starts ramping up linearly with the slope equal to Vin/Lp. The voltage induced in the secondary winding and the feedback winding make the fast recovery rectifier reverse biased and hold the conducting transistor ON. When the primary current reaches a peak value Ip, where the core begins to saturate, the current tends to rise very sharply. This

sharp rise in current cannot be supported by the fixed base drive provided by the feedback winding. As a result, the switching begins to come out of saturation.

SMPS Block Diagram:



:

Above figure shows a block diagram example of a typical SMPS with an AC Mains (line) input and a regulated DC output. The output rectification and filter are isolated from the High Frequency switching section by a high frequency transformer, and voltage control feedback is via an opto isolator. The control circuit block is typical of specialist ICs containing the high frequency oscillator, pulse width modulation, voltage and current control and output shut down sections. Whatever the purpose of a SMPS, a common feature (after conversion of AC to DC if required) is the use of a high frequency square wave to drive an electronic power switching circuit. This circuit is used to convert the DC supply into high frequency, high current AC, which by various means, depending on the design of the circuit, is reconverted into a regulated DC output. The reason for this double conversion process is that, by changing the DC or mains frequency AC to a high frequency AC, the components, such as transformers, inductors and capacitors, needed for conversion back to a regulated DC supply, can be much smaller and cheaper than those needed to do the same job at mains (line) frequency. The high frequency AC produced during the conversion process is a square wave, which provides a means of controlling the output voltage by means of pulse width modulation. This allows the regulation of the output to be much more efficient than is possible in linear regulated supplies.

Module IV: Feedback in Oscillator Circuits:

Concept of feedback :

Feedback is the process in where some portion of the output energy is transferred back and superimposed on the input. There are two types of feedback - Positive feedback & Negative feedback. Positive feedback occurs when the feedback signal is in phase with the input signal & it increases the amplitude of the input signal,

therefore increases the gain. This means that the feedback signal will add to or "regenerate" the input signal. That's why the positive feedback is also termed as regenerative feedback. Some of the examples which uses positive feedback are Oscillator, multivibrator etc.

In case of the negative feedback or degenerative feedback, the output is 180° out of phase with the input signal & reduces the gain compared to positive feedback. Negative feedback is used to improve fidelity of an amplifier by limiting the input signal. Negative feedback can also be used to increase the frequency response of an amplifier.

Negative feedback has some advantages like:

a) It improves gain stability.

b) Reduce the distortion or noise.

c) Decreases the output impedance.

d) Increases the input impedance.

e) Increases bandwidth

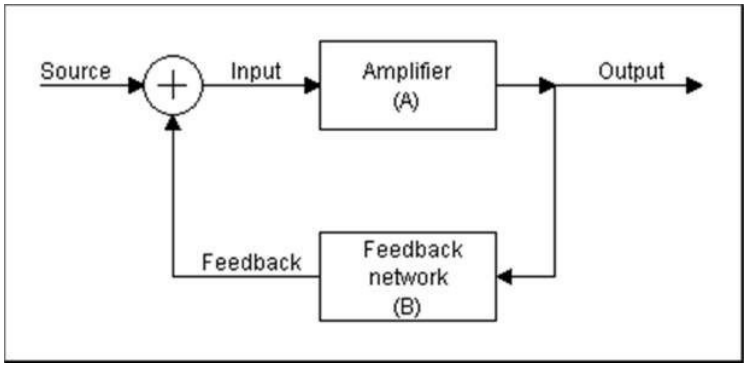
f) Increase in the range of uniform amplification.

Application of positive and negative feedback :

Due to reduced noise and distortion and increase bandwidth, the negative voltage feedback is used in radio receivers, public address system etc. Where as positive feedback is used in digital electronics to force voltages away from intermediate voltages into '0' and '1' states, loud squealing or howling sound produced by audio feedback in public address systems.

Gain calculation for positive and negative feedback :

A simple feedback loop is shown in the figure.



Feedback amplifier

The feedback amplifier consists of two blocks i.e., amplifier whose gain is A, which is the ratio of output voltage to the input voltage, i.e. $A=V_0 / V_i$

And a feedback network whose feedback factor is β, which is the ratio of feedback voltage to the output voltage i.e. $\beta = V_f / V_0$

For positive feedback, Input voltage $V_i = V_s + V_f = V_s + \beta.V_0$ (Where, V_s is the source voltage)

For negative feedback, Input voltage $V_i = V_s - V_f = V_s - \beta V_0$ (Where, V_s is the source voltage) In

case of positive feedback, the output V_0 is given by

$$V_0 = (V_s + \beta V_0)A$$

or, $V_0 (1 - A\beta) = AV_s$

So, the gain with positive feedback-

$A_f = V_0 / V_s = A / (1 - A\beta)$

In case of negative feedback, the output V_0 is given by

$$V_0 = (V_s - \beta V_0)A$$

or, $V_0 (1 + A\beta) = AV_s$

So, the gain with negative feedback-

$A_f = V_0 / V_s = A / (1 + A\beta)$

<u>Feedback topologies :</u>

There are four different types of feedback topologies depending on the input signal (voltage or current) to be amplified and form of the output signal (voltage or current).

Topologies are (i) Voltage-Series feedback (ii) Current Series Feedback (iii) Voltage shunt feedback (iv) Current shunt feedback

Usually the 1st term in feedback topology indicates the sampling term and 2nd term indicates mixing term.

The different types of feedback topology is described below-

a) Voltage-series:

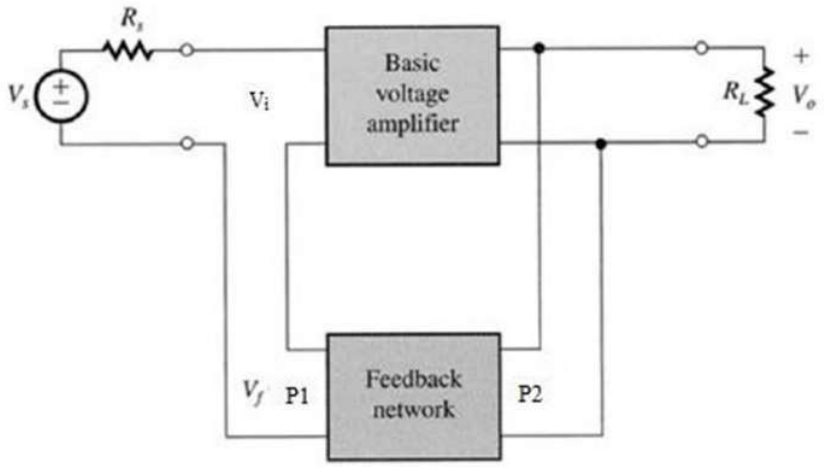


Fig.2 Voltage series feedback configuration

Here both the output signal and the feedback signal are voltage signal and the voltage is feedback to the input in series. Therefore, it is also called as shunt-series feedback. It provides high input impedance and low output impedance. In above fig port 1 refers the output of feedback network where as port 2 refers the input of feedback network. This type of feedback topology is used in voltage amplifiers.

b) Current series:

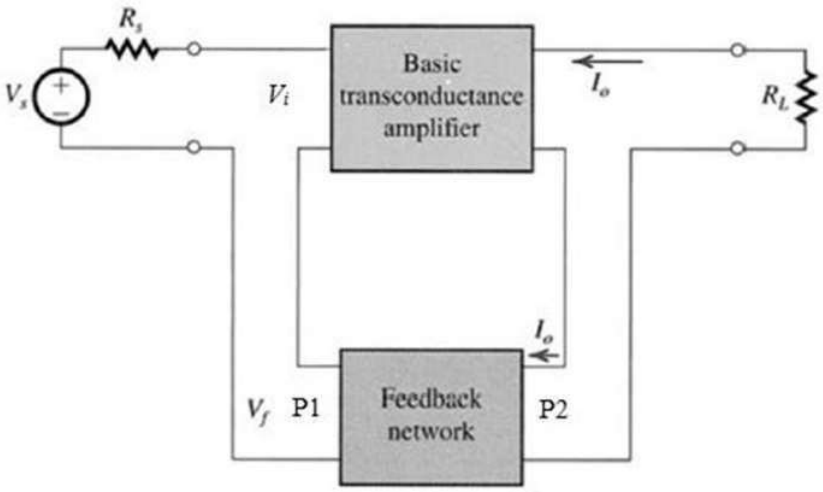
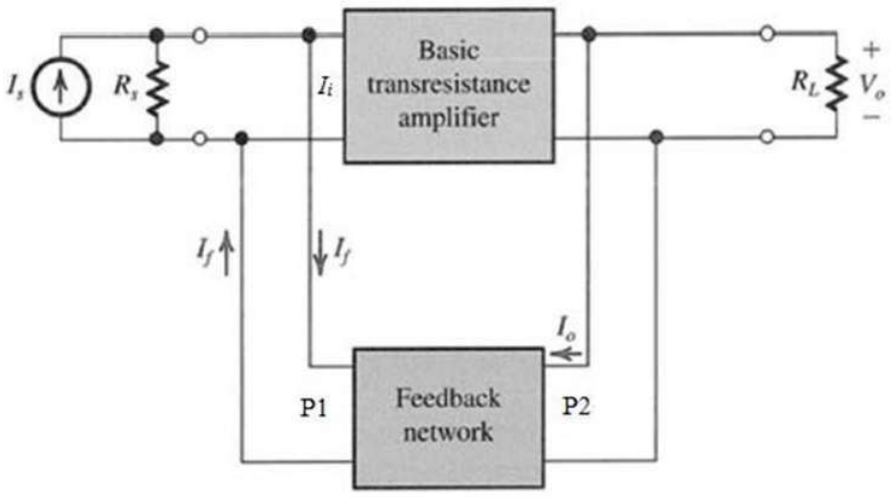


Fig.3 Current series feedback configuration

Here, the output signal is current signal, but the feedback signal is voltage signal and the voltage is feedback in series to the input. Therefore, it is also called as series-series feedback. This employed high input and output impedance. In fig. port 1 refers the output of feedback network where as port 2 refers the input of feedback network. This type of feedback topology is used in trans-conductance amplifiers.

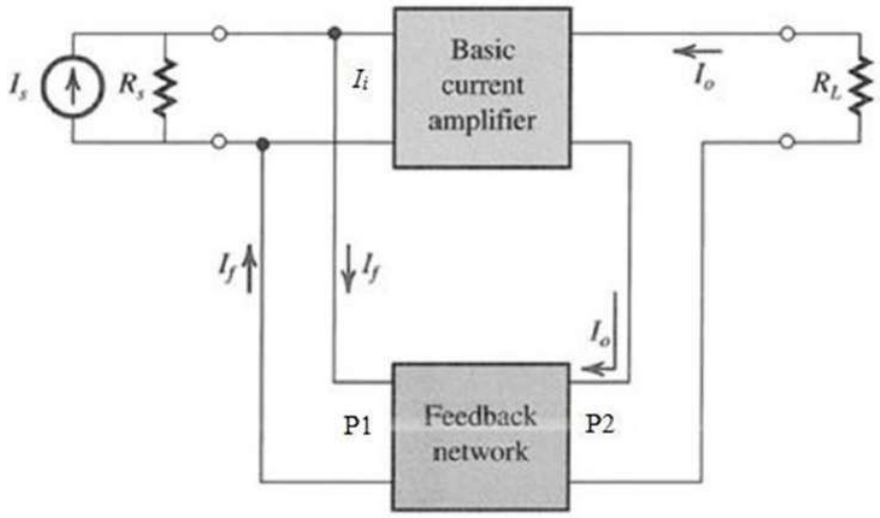
c) Voltage shunt:



Voltage shunt feedback configuration

Here the output signal is voltage signal, but the feedback signal is current signal. Therefore, it is also called as shunt-shunt feedback. In the fig port 1 refers the output of feedback network where as port 2 refers the input of feedback network. This provides low output impedance and high input impedance. This type of feedback topology is used in trans resistance amplifier.

d) Current shunt:



Current shunt feedback configuration

Here both the output signal and the feedback signal are current signal. The current is feedback in shunt to the input. Therefore, it is also called as series-shunt feedback. In above fig port 1 refers the output of feedback network where as port 2 refers the input of feedback network. It provides high input and low output impedance. This type of feedback topology is used in current amplifiers.

Berkhausen criterion:

It is already discussed that the voltage gain of a positive feedback amplifier is given by

$$A_f = V_0 / V_s = A / (1 - A\beta)$$

Where, A is the open loop gain of the amplifier. If a circuit is designed using positive feedback, so that

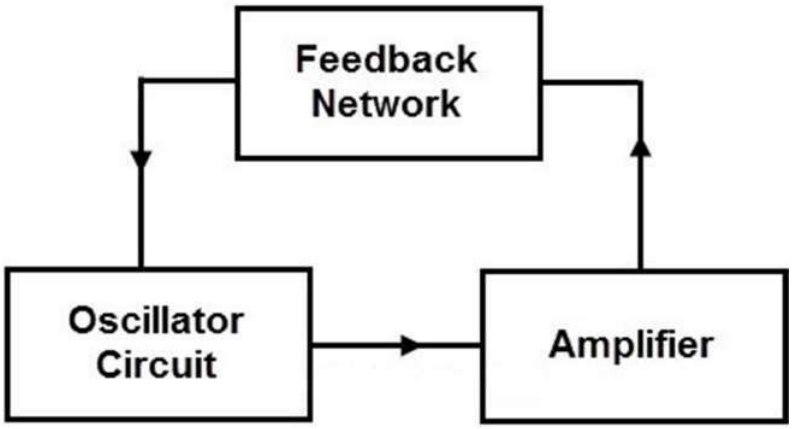
$$A\beta = 1$$

then the closed loop gain (A_f) would be infinite. The amplifier then delivers an output even with zero input voltage, i.e. the amplifier becomes an oscillator (the overall phase shift of the feedback is 360◦). The condition of unity loop that is, $A\beta = 1$ is called Berkhausen criterion.

Concept of Oscillator :

An electronic circuit used to generate the output signal with constant amplitude and constant desired frequency is called as an oscillator. It is also called as a waveform generator which incorporates both active and passive elements.

The primary function of an oscillator is to convert DC power into a periodic signal or AC signal at a very high frequency. An oscillator does not require any external input signal to produce sinusoidal or to start or maintain the conversion process. As long as the DC power is connected to the oscillator circuit, it keeps on producing an output signal with frequency decided by components in it.



Block diagram of oscillator

The above figure shows the block diagram of an oscillator. An oscillator circuit uses a vacuum tube or a transistor to generate an AC output.

The output oscillations are produced by the tank circuit components either as R and C or L and C. For continuously generating output without the requirement of any input from preceding stage, a feedback circuit is used.

From the above block diagram, oscillator circuit produces oscillations that are further amplified by the amplifier. A feedback network gets a portion of the amplifier output and feeds it the oscillator circuit in correct phase and magnitude.

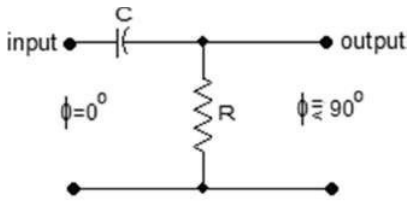
Classification of oscillator Circuit:

Feedback oscillator circuits can be classified according to the type of frequency selective filter they use in the feedback loop.

- RC Oscillator: In this oscillator the filter is a network of resistors and capacitors. RC oscillators are mostly used to generate lower frequencies, for example in the audio range. Common types of RC oscillator circuits are the phase shift oscillator and the Wien bridge oscillator.

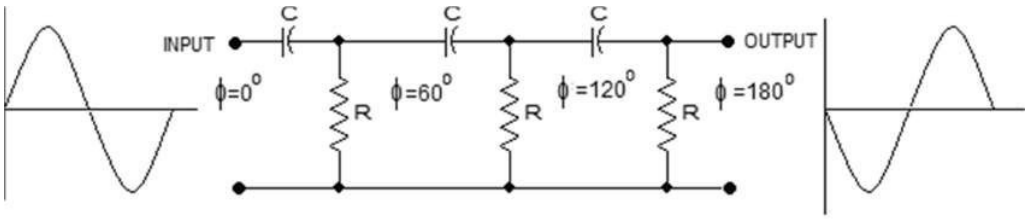
Phase Shift Oscillator:

RC phase shift network is a simple resistor capacitor network that can be used to give a desired phase shift to a signal. The circuit diagram of a simple single stage RC network is shown in the figure below



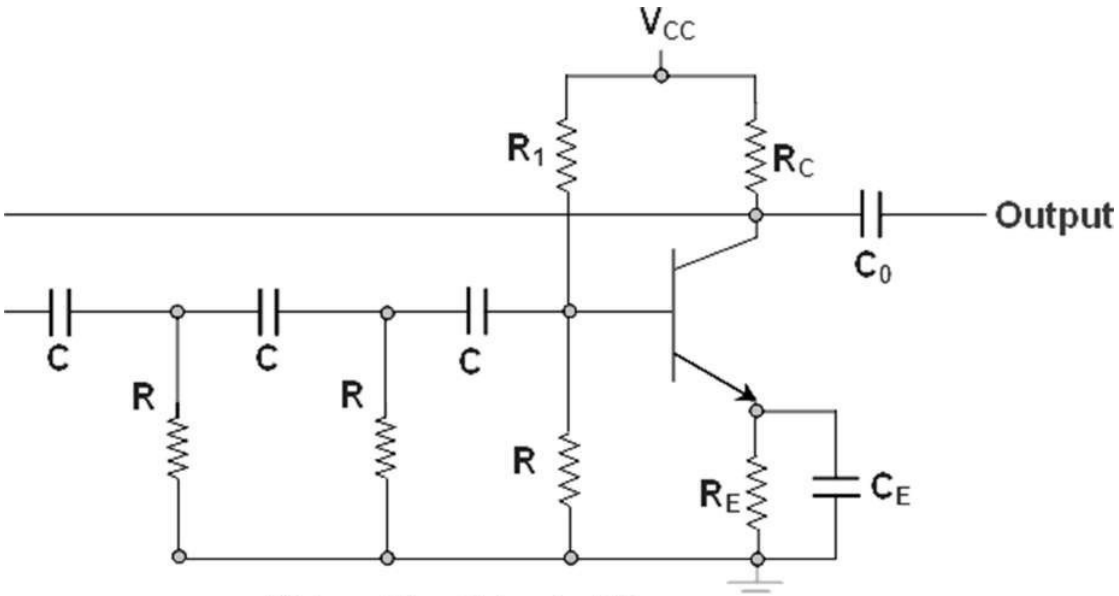
Single stage RC phase shift network

Theoretically in a simple RC circuit , the output voltage will lead the input voltage by a phase angle $\Phi = 90°$. But practically the phase angle will be less than 90°, because it is impossible to get a ideal capacitor. Phase shift of a practical RC network depends on the value of the capacitor, resistor and the operating frequency. So, RC phase-shift oscillator is formed by cascading three RC phase-shift networks, each offering a phase-shift of 60°, as shown by Figure



3 stage RC phase shift network

Using this RC phase shift network transistor based RC phase shift oscillator can be made, which is shown below-



RC phase-shift oscillator using BJT

Here the collector resistor RC limits the collector current of the transistor, resistors R1 and R (nearest to the transistor) form the voltage divider network while the emitter resistor RE improves the stability. Next, the capacitors CE and Co are the emitter by-pass capacitor and the output DC decoupling capacitor, respectively. Further, the circuit also shows three RC networks employed in the feedback path. This arrangement causes the output waveform to shift by 180° during its course of travel from output terminal to the base of the transistor. Next, this signal will be shifted again by 180° by the transistor in the circuit due to the fact that the phase-difference between the input and the output will be 180° in the case of common emitter configuration. This makes the net phase-difference to be 360°, satisfying the phase- difference condition. One more way of satisfying the phase-difference condition is to use four RC networks, each offering a phase-shift of 45°. Hence it can be concluded that the RC phase-shift oscillators can be designed in many ways as the number of RC networks in them is not fixed. However it is to be noted that, although an increase in the number of stages increases the frequency stability of the circuit, it also adversely affects the output frequency of the oscillator due to the loading effect. The generalized expression for the frequency of oscillations produced by a RC phase-shift oscillator is given by

$f = 1/2\pi RC\sqrt{2N}$

Where, N is the number of RC stages formed by the resistors R and the capacitors C. Ignoring

loading effects, β can be calculated over the feedback network, and is given by:

$\beta = V_i / V_o = 1/\ 1 - 5/(\omega RC)^2 + j(1/(\omega RC)^3 - 6/\omega RC)$

For a phase shift of 180º, the imaginary part is zero, which leads to

$\omega_0 = 1/\sqrt{6}RC$

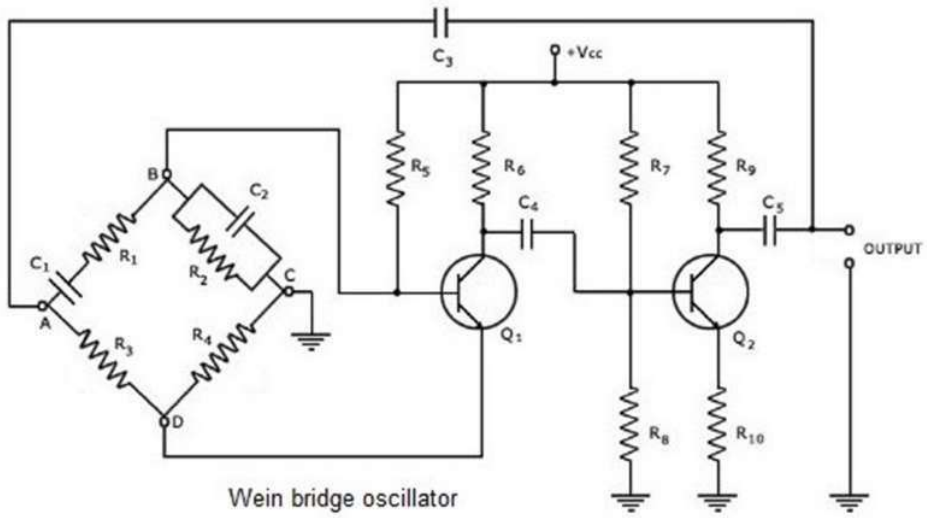
Then, $\beta = -1/\ 29$

and the gain required by the Barkhausen criterion is

$A = 1/\beta = -29$

Wien bridge oscillator

The Wien Bridge Oscillator is so called because the circuit is based on a frequency-selective form of the Wheatstone bridge circuit. The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillator.



Wein bridge oscillator

From the above diagram we can see the two transistors are used for giving the phase shift of 360°, which is required for the positive feedback. The base current is applied to the collector terminal of the first transistor and the phase shift is about the 180°. The output of the first transistor is given to the base terminal of the

second transistor Q2 with the help of the capacitor C4. Further, this process is amplified and from the second transistor of collector terminal the phase reversed signal is collected. The frequency selective RC network does not produce any phase shift. The condition for sustained oscillation is-

$X_c = R$

Where, Xc= Capacitive reactance = $1/ 2\pi fc$

R = Resistance of resistors

So, $1/ 2\pi f_c = R$

The frequency of oscillation of Wien Bridge oscillator is- f =

$1/ 2\pi\sqrt{R_1R_2C_1C_2}$

Where, $R_1 = R_2 = R$

And, $C_1 = C_2 = C$

Then, $f = 1/ 2\pi RC$

At this frequency feedback factor $\beta = 1/3$

Since, for $A\beta \geq 1$, $A \geq 3$

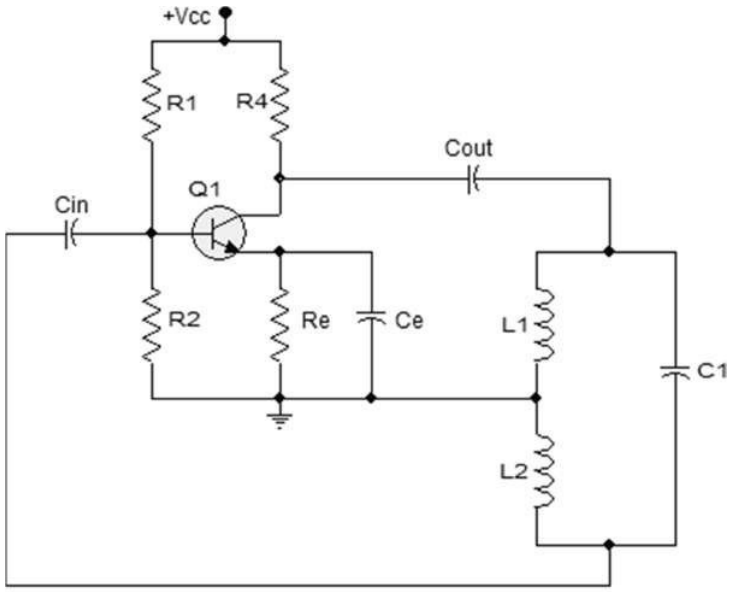
That is, gain of amplifier must be greater than or equal to 3.

- LC Oscillator: In an LC oscillator circuit, the filter is a tuned circuit consisting of an inductor(L) and capacitor (C) connected together. LC oscillators are often used at radio frequencies, in signal generators, tunable radio transmitters and the local oscillators in radio receivers. Typical LC oscillator circuits are the Hartley and Colpitts oscillator.

  Hartley Oscillator :

  The Hartley oscillator is modified version of the Tuned base oscillator. It is widely used in local oscillator in radio receivers. It can generate wide range of high frequency (20KHz to 30MHz) and it is easy to tune.

  The circuit diagram of Hartley oscillator is shown in the following fig. It consist of common emitter amplifier which produces 180º phase shift and a tank circuit with capacitor C and split inductor in feedback. The tank circuit produces 180º phase shift for higher frequency. Voltage divider formed by the resistances R1 and R2 maintains the biasing of transistor. Re is the emitter resistor, which provide thermal stability for the transistor. Ce is the emitter by pass capacitors,
  which by-passes the amplified AC signals. If the emitter by-pass capacitor not there, the amplified ac voltages will drop across Re and it will get added on to the base-emitter voltage of Q1 and will disrupt the



Hartley oscillator

biasing conditions. C_{in} is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage.

The frequency "F" of a Hartley oscillator can be expressed using the equation;

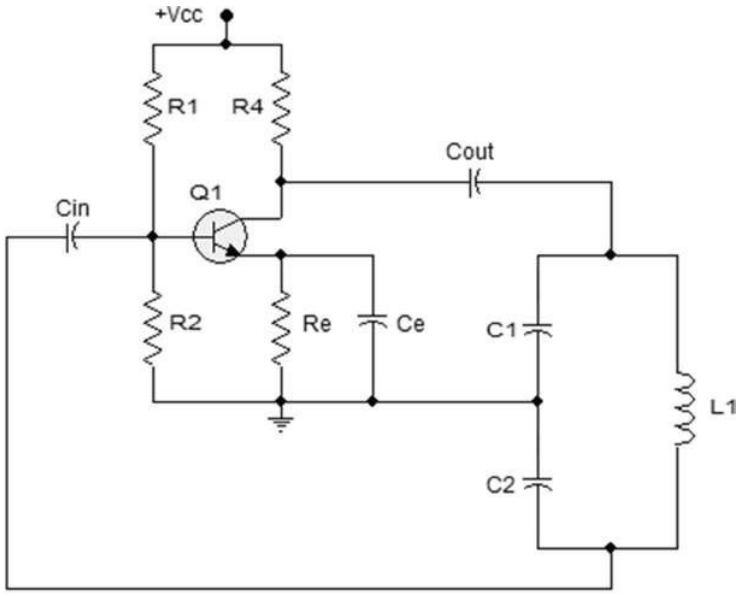
$$f = 1/2\pi\sqrt{LC}$$

Where, C is the capacitance of the capacitor C_1 in the tank circuit.
And $L = L_1+L_2$, the effective series inductance of the inductors L_1 and L_2 in the tank circuit.

Here the coils L_1 and L_2 are assumed to be winded on different cores. If they are winded on a single core then $L = L_1+L_2+2M$, where M is the mutual inductance between the two coils.

Colpitts oscillator :

Collpitts oscillator is generally used in RF applications and the typical operating range is 20 KHz to 300 MHz. In Colpitts oscillator, the capacitive voltage divider is used in the tank circuit. The circuit diagram of Colpitts oscillator is shown in the figure below.



Colpitts oscillator

Here the resistors R_1 and R_2 is used as a voltage divider biasing to the transistor. Resistor R_4 limits the collector current of the transistor. Cin is the input DC decoupling capacitor while Cout is the output decoupling capacitor. R_e is the emitter resistor which is used for thermal stability. C_e is the emitter by- pass capacitor, which by-pass the amplified AC signals, dropping across R_e. If the emitter by-pass capacitor is not there, the amplified AC signal will drop across Re and it will alter the DC biasing conditions of the transistor, and the result will be reduced gain. Capacitors C_1, C_2 and inductor L_1 forms the tank circuit. The resonant frequency of the Colpitts oscillator is given by-

$$fr=1/(2\Pi\sqrt{(L1*C)})$$

Where fr is the resonant frequency

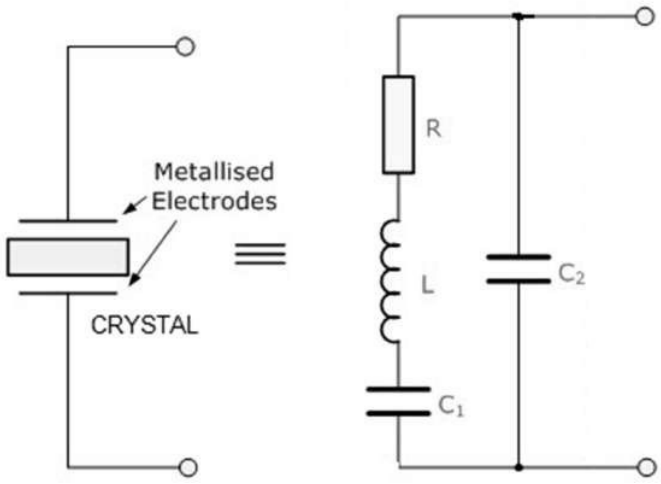
C is the equivalent capacitance of series combination of C1 and C2 of the tank circuit

It is given as, $C= (C1*C2)/((C1+C2))$

L1 represents the self inductance of the coil.

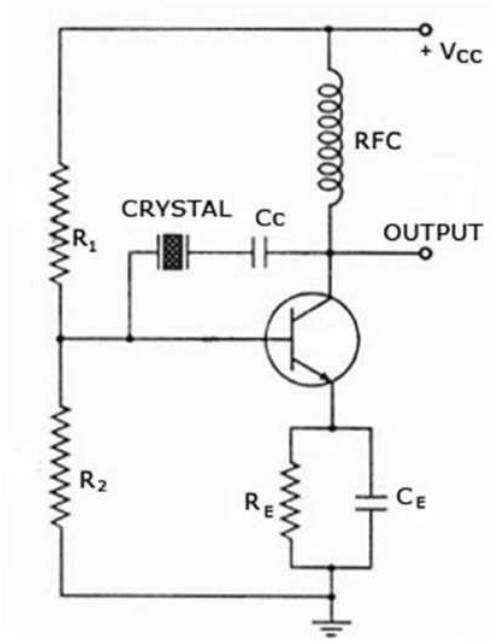
- Crystal Oscillator: In a crystal oscillator circuit the filter is a piezoelectric crystal (commonly a quartz crystal). The crystal oscillator is basically a tuned oscillator as the voltage and current are in same phase. When an ac voltage is applied across an crystal, it starts vibrating at the frequency of supply

voltage, the effect is known as piezoelectric effect and the crystal which exhibit this effect is known as piezoelectric crystal. The crystal oscillator provides a high degree of frequency stability and accuracy. So, these are very useful in those applications where frequency stability is very essential. The crystal oscillators are widely used in communication, transmitter, digital watches and clocks.

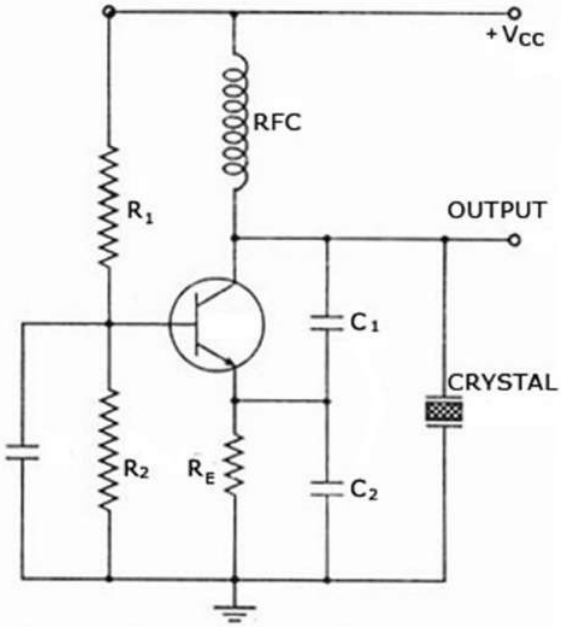


Electrical equivalent circuit of quartz crystal

In crystal oscillators, the crystal is mounted between two metal plates, Although the crystal has electro-mechanical resonance but the crystal action can be represented by an electrical resonance circuit, as shown in fig. The crystal actually behaves as a series R-L-C circuit in parallel with C_M where C_M is the capacitance of the mounting electrodes. Because of presence of C_M, the crystal has two resonant fre- quencies. One of these is the series resonant frequency f_s at which the crystal impedance is very low. The other is parallel resonance frequency f_p which is due to parallel resonance of capacitance C_M and the reactance of the series circuit. In this case crystal impedance is very high. The series resonant frequency is given by – $f_s = 1/2\ \pi\ \sqrt{LC}$ and, the Parallel resonant frequency is given by- $f_p = 1/2\pi\sqrt{[L(C_MC/C_M+C)]}$



Oscillator with crystal operating in series resonance



Oscillator with crystal operating in series resonance

It appears that f_p is higher than fs but the two frequencies are very close to each other. It is due to the fact that the ratio C/C_M is very small. To stabilize the frequency of an oscillator, a crystal may be operated at either its series or parallel resonant frequency.

Module V: Operational amplifier:

Ideal op-amp characteristics

The ideal op-amp is characterized by seven properties:

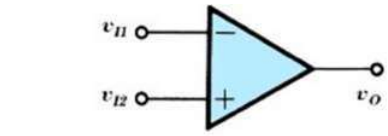
Infinite open-loop voltage gain
Infinite input impedance Zero
output impedance
Zero noise contribution
Zero DC output offset
Infinite bandwidth
Differential inputs that stick together

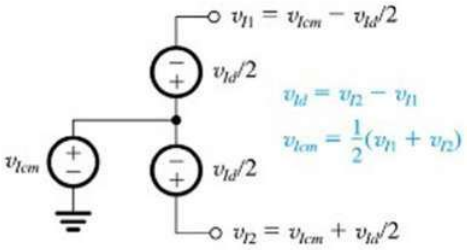
Differential amplifier

Difference amplifier

- Ideal difference amplifier:
  - Responds to differential input signal v_{Id}
  - Rejects the common-mode input signal v_{Icm}
- Practical difference amplifier:
  - $v_O = A_d v_{Id} + A_{cm} v_{Icm}$
    - → A_d is the differential gain
    - → A_{cm} is the common-mode gain
  - Common-mode rejection ratio (CMRR):

$$CMRR = 20\log\frac{|A_d|}{|A_{cm}|}$$





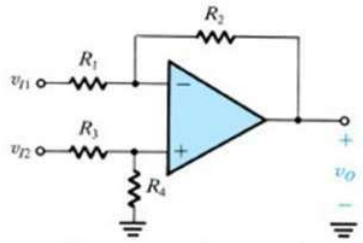
Single op-amp difference amplifier

$$v_+ = \frac{R_4}{R_3 + R_4} v_{I2} = v_-$$

$$v_O = v_- + iR_2 = v_- + \left(\frac{v_- - v_{I1}}{R_1}\right)R_2 = -\frac{R_2}{R_1}v_{I1} + \frac{1 + R_2/R_1}{1 + R_3/R_4}v_{I2}$$

$$= -\frac{R_2}{R_1}(v_{Icm} - v_{Id}/2) + \frac{1 + R_2/R_1}{1 + R_3/R_4}(v_{Icm} + v_{Id}/2)$$

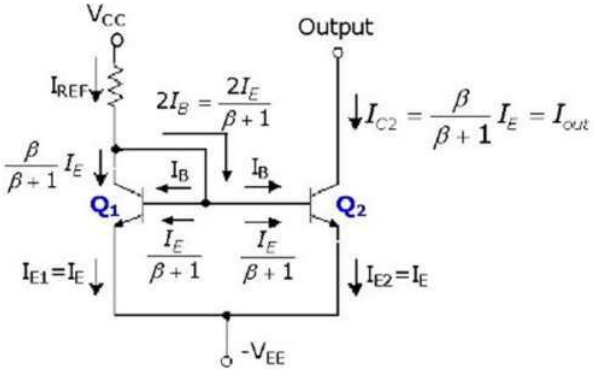
$$= \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1}\right)v_{Icm} + \frac{1}{2}\left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1}\right)v_{Id}$$



$$A_d = \frac{1}{2}\left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1}\right) \qquad A_{cm} = \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1}\right)$$

Constatnt Current Source(Current Mirror)

The most basic building block in the design of IC current sources, also known as the **current mirror**, is shown in the figure to the right (a modified version of Figure 5.27 in your text). The transistors, Q_1 and Q_2, are matched devices with their bases



and emitters tied together. The transistor designated Qm in the figure is connected as a diode by sho rting its base and collector terminals.

A reference current, IREF. is the input to the current mirror at the collector of the diode-connected transistor Qi and the output is taken from the collector of Q . Note: Q must remain in the active (linear) region of operation by keeping its collector voltage higher than the base voltage at all times. It is important that the loading effect of any circuit fed by this current mirror should be inspected to ensure maintaining this mode of operation.

The key point to the analysis of the current mirror circuit is that the transistors are matched and have the same VeE Using this and examining the circuit above, the inp ut current I REF flows through Q and sets up a voltage across Q1. This voltage then appears across the base and emitter of Q since the devices are connected in parallel. Assuming the assumption I c- IE iS valid (p §+1), and using the fact that the transistors are matched, the emitter currents of Qm and Qm are the same and equal to IxEF. As long as Q remains in the active region of operation, the output current, I ut, \ñ/III also be approximately equal to UEFA

If the effect of finite § is considered, the currents are as indicated in the figure above. This may lead to an output current that is not equal to the input reference current, since

$$/ \qquad \frac{\beta}{\text{p+1}} I_E \text{ and } I_{,,} \qquad \frac{\text{p+2}}{\text{p+1}} \; {}_{Ei} \qquad \text{(Equations 5.59 \& 5.60)}$$

where the expression for IREF is found by using KCL at the collector of Qi.
The current gain of the current mirror is

$$\frac{}{I_{REF}} \quad \frac{}{\beta + 2'}$$

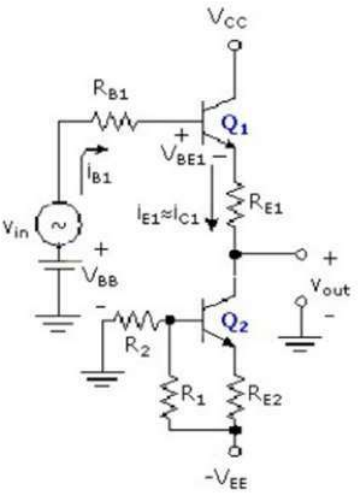
which approaches unity for § very large. Another deviation of tout from I «EF has to do with the Early effect. Since the VIE of Q is constant as determined by IREF. the output resistance of Qz determines the dependence of Iout• ThIS may be perceived as a disadvantage of this configuration - the output resistance of the current mirror (called Rs in your text) is limited by the ro of Q_2, or

$$0 \text{ "} \quad \frac{V_A}{\text{out}} \quad \frac{V_A}{9EF \text{ "}}$$

LEVEL SHIFTER

As mentioned in the previous section, we often assume perfect symmetry and ideally matched devices for differential amplifiers so that the differential common mode output is exactly equal to zero. However (and big surprise), even if the input average value is zero volts, the amplifier output may have a non-zero average voltage due to biasing effects. These offsets appear as dc voltages, usually quite small, and may be of little concern for a simple amplifier. The problem arises when a high gain multi-stage dc amplifier, such as an operational amplifier, encounters these offset voltages. Since the gain of the op-amp is so high, a small offset in one of the earlier stages may propagate through the system and saturate a later stage. This leads to all kind of ugly things – most noticeably an output that may be totally worthless! So… to solve this dilemma, we need something that will give us unity gain for ac signals while allowing us to compensate (add or subtract) a dc voltage to remove the unwanted offset.

The circuit shown to the right is a modified version of Figure 9.7b in your text. Transistor Q_2 forms a constant current source as well as providing an additional resistance in the emitter circuit of Q_1 (Note: any of the current sources of section G2 may be used). With this in mind, transistor Q_1 is configured as an emitter-follower amplifier stage that acts as a level shifter. This level shifter acts as a unity gain amplifier for ac signals while providing an adjustable dc output.



For the dc portion of the analysis, the ac signal (v_{in}) is ignored and a KVL is written about the base-emitter loop of Q_1:

For the dc portion of the analysis, the ac signal (v_{in}) is ignored and a KVL is written about the base-emitter loop of Q_1:

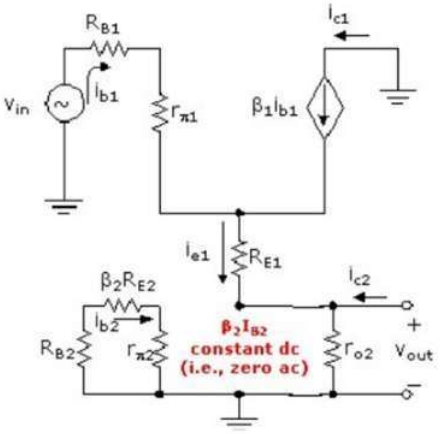
$$V_{BB} = I_{B1}R_{B1} + V_{BE1} + I_{E1}R_{E1} + V_{out},$$

where V_{BB} is the dc level acquired from a previous stage and $R_B=R_1||R_2$. Using the relationship $I_B=I_C/\beta$ and assuming that $I_E\approx I_C$, Equation 9.34 may be solved for the dc value of the output voltage as

$$V_{out} = V_{BB} - I_{C1}\left(\frac{R_{B1}}{\beta} + R_{E1}\right) - V_{BE}.$$

All the parameters in the right hand side of Equation 9.36 are fixed or previously defined except for the value of R_{E1}. By varying R_{E1}, the dc level of the output voltage may be set to any desired value less than V_{BB}-V_{BE} (this is assuming that $I_{C1}R_B/\beta$ is very small). The level shifter illustrated above is used to shift the output **downward** to a lower value. If **upward** shifting is required, the same circuit is used, but pnp transistors are substituted for the npn transistors.

Figure 9.7c, modified and reproduced to the right, is the mid-frequency small signal model of the circuit above. Note that since $\beta_2 I_{B2}$ (the collector current of the current source) is assumed to be a constant dc value, it is an open circuit for ac conditions. In the following discussion, we are going to be assuming that β_1 and β_2 are very large, so that



$$i_{e1} \cong i_{c1} = \beta_1 i_{b1} \cong i_{c2} = \frac{v_{out}}{r_{o2}}.$$

Using KVL, we can write the ac equation of the level shifter as

$$v_{in} = i_{b1}R_{B1} + i_{b1}r_{\pi 1} + i_{e1}R_{E1} + v_{out}.$$

Using the approximations above, we can express the currents of Equation 9.37 as follows:

$$i_{e1} = \frac{v_{out}}{r_{o2}} \quad \text{and} \quad i_{b1} = \frac{v_{out}}{\beta_1 r_{o2}}.$$

Substituting these expressions into Equation 9.37, we can express the ac KVL in terms of circuit components, physical parameters and input and output voltages as

$$v_{in} = \frac{R_{B1}v_{out}}{\beta_1 r_{o2}} + \frac{r_{\pi 1}v_{out}}{\beta_1 r_{o2}} + \frac{R_{E1}v_{out}}{r_{o2}} + v_{out}$$

$$= v_{out}\left(\frac{R_{B1} / \beta_1 + r_{e1} + R_{E1}}{r_{o2}} + 1\right)$$

(Equation 9.38, Modified)

where $r_{\pi 1}/\beta_1$ has been replaced by r_{e1}. The voltage gain is the ratio of ac output to ac input, or

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + (R_{B1} / \beta_1 + r_{e1} + R_{E1}) / r_{o2}} = \frac{r_{o2}}{r_{o2} + (R_{B1} / \beta_1 + r_{e1} + R_{E1})} \quad \text{(Equation 9.39, Modified)}$$

As r_{o2} becomes very large (which is a characteristic of several of the current sources we discussed), the gain of Equation 9.39 approaches one and the level shifter behaves as an emitter follower for ac signals – which is what we wanted, so this is good!

Common Mode Rejection Ratio

In general, an instrumentation amplifier is required to amplify the difference between two input signals or voltages, V_1 and V_2 as shown in Fig.1. However, as discussed, in the case of many transducers there is often a potential at both inputs present when the input parameter to be measured is zero. This signal is the same at both inputs and is present regardless of the value of the input parameter. This signal is defined as the *Common-Mode* input signal, V_{ic} and should make no contribution to the output voltage of the amplifier. On the other hand, when the value of the input parameter is non-zero, the potential at one input terminal will increase, while that at the other input terminal will decrease proportionately, giving a difference in the potentials at the two input terminals. This difference in the two input potentials is defined as the *Differential-Input* signal, V_{id}. Fig. 1 below shows the common-mode voltage as applied centrally to both input terminals of the amplifier while the differential voltage is considered split between the two inputs as half the differential potential one each side, V_{id} /2. It is applied as a positive sense signal to the non-inverting input of the amplifier and as a negative sense signal to the inverting input of the amplifier.

V,g/ 2

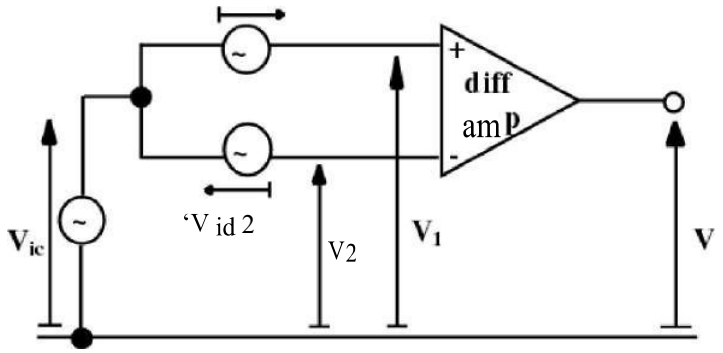


Fig. 1 Differential and Common diode Inputs to a Differential Amplifier

This distribution of common-mode and differential mode signal is illustrated in Fig, 2. The potentials show'n represen t steady-state or dc levels, but could equally be time-i arring or dynamic signals. For example if the signal of interest to be measured were the Electr ocardiogram obtained from two electrodes placed on the surface of the body, then this w'ould form the differential input signal. The common-mode signal in this scenario is onen composed of mains interference from the electricity supply. This gis es rise to an unwanted sienal at the innut of the amnlifier w'hich must be rejected in favour of

the w'anted differential signal w'hich should be amplified. The ability of the amplifier to d iscriminate against the common- mode signal and prevent it from making any contribution to the output voltage of the amplifier is termed

Common diode Re(ection Id cally, the common-mode input signal should produce no response at the output but in practice it does make some contribution. A figure of merit used to quantiJ the extent of an amplifier's abilip to reject or supress the common-mode input signal is the Common -ñIode-Rejection-Ra tio or ChlRR of the amplifier.

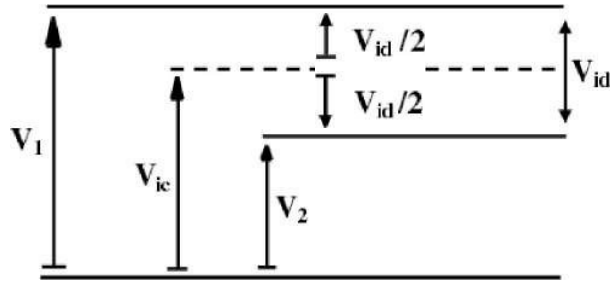


Fig. 2 The Distribution of Differential and Common diode Input Voltages

From the aboi e definitions and from Fig. 1 and Fig. 2 w'e hat e:

I ' ‹r 2 and 2 ' ie " 2

so that:

$$V_{id} = V_1 - V_2 \quad \text{and} \quad V_{ic} = \frac{V_1 + V_2}{2}$$

If the differential amplifier w'ere ideal, it would suppress the common-mode componen t of the input signal so that the output has no contribution from the common mode input and the ootput i oltage would be simply be gis en bj.-

$$V \quad A_d (V, — V_2) \; A_d V_{i\,d}$$

w'here At is the differential gain of the amplifier as gis en, for example by Eq. 6 of the previous lecture. However, in practice the amplifier does not fully reject the common mode componen t of the input signal and this consequen tly makes some contribution to the output. A common-mode gain, @ can therefore also be sliecified so that the output i oltaee of the amlilifier is cii en in liractice as:

IdeaMv — Obmtin pracGceA mcA bmtisfinite.

The measure of the abiliy' of the amplifier to reject the common mode input component ie , in favour of the differential component is the Common-Plod e- Rejection Ratio or CñlRR of the amplifier. This is defined as:

$$\text{CMRR} = \frac{A}{—} \quad ; \quad \text{ideally } A, \quad 0 \quad \text{and CIYIRR}$$

Then expressing the common-mode gain in terms of the d ifferential gain w'e have:

$$e - \frac{}{\text{CMRR}}$$

In this case: A_d

$$\text{t o'} \quad A_d V_d + \frac{}{} V$$

CMRR '*

The len hand term is the wanted output signal while the right hand term is essentially an error component. The error in the output is then gis en as the ratio of these componen ts:

$$\varepsilon = \frac{V_{ic}/CMRR}{V_{id}} = \frac{1}{CMRR}\frac{V_{ic}}{V_{id}} \text{ x } 100\,\%$$

In order to obtain a desired fractional error ε the required CMRR is:

$$CMRR = \frac{1}{\varepsilon}\frac{V_{ic}}{V_{id}}$$

For example, if V_{ic}=1V and V_{id} =1mV, then for a 1% error we need:

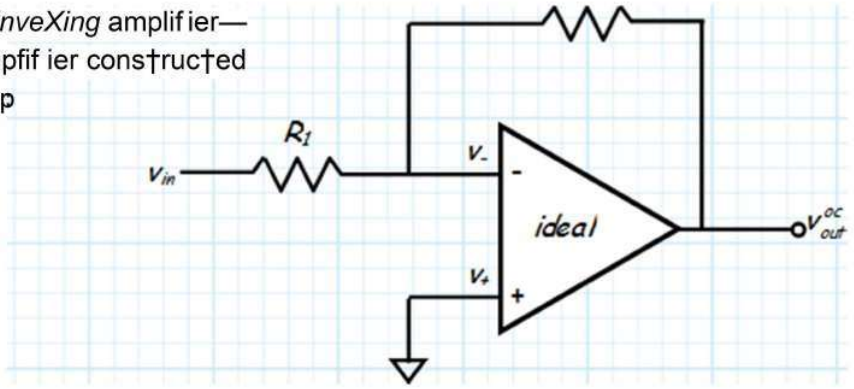
$$CMRR = \frac{1}{0.01} \text{ x } \frac{1}{10^{-3}} = 10^5 \equiv 100\text{dB}$$

This is substantial but typical of the CMRR required in bio-amplifiers.

Open & closed loop circuits

Closed-Loo p and Open-Loop Gain

Cons ider †h e *inveXing* amplif ier—a 'faadbock ampfif ier cons†ruc†ed wi†h an o p-amp



Th e opan-circuit vo f†age gain of †h is ampfif ier:

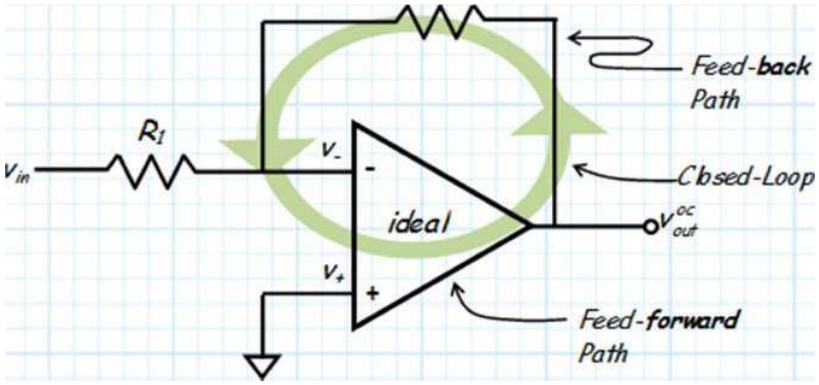
—

A closed loop

Q: *Closed loop? What does that mean?*

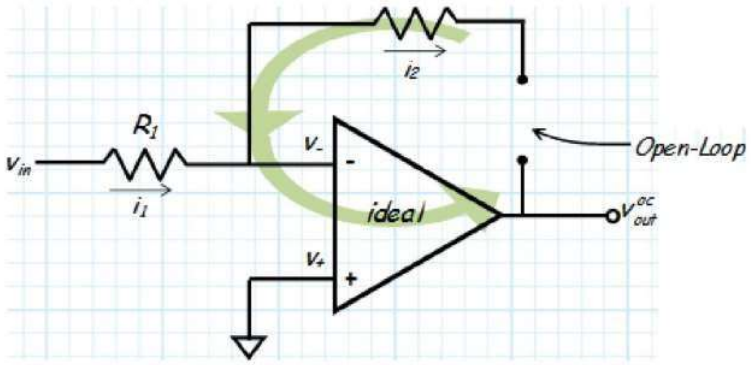
A: Th e †erm "c hosed loop" refers †o loo p formed by †h e {aed-{orwor'd | z†h and the faed -beck (i.e., feed back) [xtth of †h e amp Gif ier.

In †h is case, †h e food- srwor'd |xtth is formed by †h e op -amp, wh ice †h e faod- beck |xtth is formed by †h e feedback imsisfor Ay



An open loop

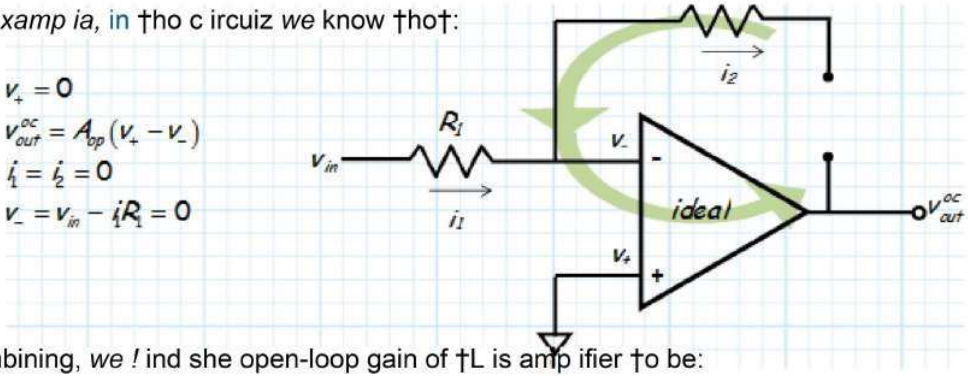
Zf the loop is brokan, †han *we say* †he loop *is* "open". Tha gain (v„'v,) for he open loop case ir nzfernzd †o as †he open-loop gain.



Open and closed loop gains

for axamp ia, in †ho c ircuiz *we* know †ho†:

$$v_+ = 0$$
$$v_{out}^{oc} = A_{op}(v_+ - v_-)$$
$$i_1 = i_2 = 0$$
$$v_- = v_{in} - i_1 R_1 = 0$$



Combining, *we !* ind she open-loop gain of †L is amp ifier †o be:

$$A \quad \frac{v_{out}^{oc}}{}$$

Once *we* "c lose" †h s loop, *we* hove on ornpfif ier *wi†h* a closed-loop *gain:*

$$A_{closed} = \frac{v_{out}^{oc}}{} = -\frac{R_2}{}$$

u/h ich al course is †h e opan-ciz•cuif voltage gain of †h *is inventing* amplif ier.

Feedback is a wonderful †hing

hbte that 4he clasad-bop gain (—@/) does not expiic”rtly involve tke op-amp gain A

” The closed-kop gain is determined by two r•esls'tow clues. which typically are selected †o provide s ifizarr gain ((@(> 1). albeit not so large that the amplifier is easily sehum3od.

” 6onverseJy. the opan-loop gain (-A obviously does involve the op-amp gain. Moreover. as in this case. the open-loop gain of a feedl>zck am|difier often only involves the op-amp gain!

” As a result. the op-exp goes is often altermtively nsferrad to as the

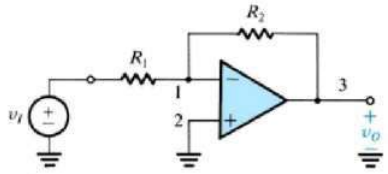
hbte that doing the feedback loop turns a generally useless amplifier (the gain is too high!) into a var•y useful one (the gain is just right}

---

gur

The inverting close-loop coiifiguratxon

O External components R, a net fl, form a close loop
O Output is fed back to the inverting input terminal
O Input signal is applied horn the irn=ertirtg terminal



Inverting-coiifigviratiou usiiip ideal op amp

OThe required conditions to apply virtu aI short for op-amp circuit,
M Negative feedback cnnfiguration
■ Ixifizxite open-lonp gain

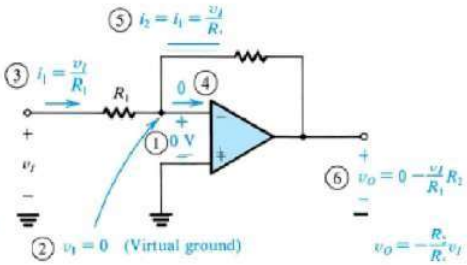
ISO S.'£• -)O O gd iO: — VO/Y1 ' 'z ;'

- Infinite differential g•ain: v, — r, = vp ,'r1 = o
- ■ Infinite input impedance: i, = i, = o
- Zero ourput impedance: rp = v, — ill, = — vj fi_ ,'R,
- Voltage gain is negatis-e

R Inp ut a net output signals are out of phase

- Closed-loop gain clepends entsely on external passive components Imdepenclent of op-amp g•ain)

M Close-loop amplifier trades gain (hip•h open-loop p•ain) for accuracy (finite but accurate closest-loop gain)



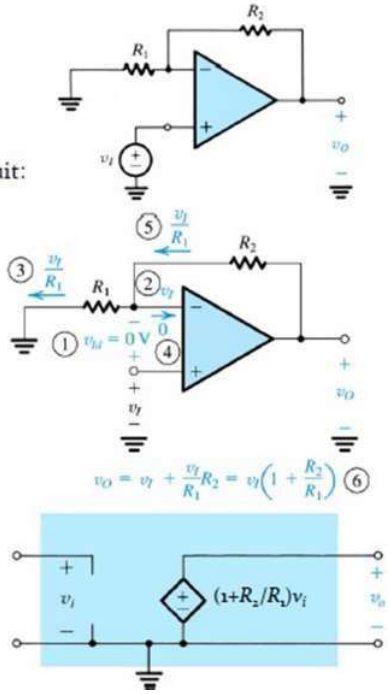
Noninverting Configuration

The noninverting close-loop configuration

- External components R_1 and R_2 form a close loop
- Output is fed back to the inverting input terminal
- Input signal is applied from the noninverting terminal

Noninverting configuration using ideal op amp

- The required conditions to apply virtual short for op-amp circuit:
  - **Negative feedback configuration**
  - **Infinite open-loop gain**
- Closed-loop gain: $G \equiv v_O/v_I = 1 + R_2/R_1$
  - Infinite differential gain: $v_+ - v_- = v_O/A = 0$
  - Infinite input impedance: $i_2 = i_1 = v_-/R_1$
  - Zero output impedance: $v_O = v_- + i_1R_2 = v_I(1 + R_2/R_1)$
  - Closed-loop gain depends entirely on external passive components (independent of op-amp gain)
  - Close-loop amplifier trades gain (high open-loop gain) for accuracy (finite but accurate closed-loop gain)
- Equivalent circuit model for the noninverting configuration
  - Input impedance: $R_i = \infty$
  - Output impedance: $R_o = 0$
  - Voltage gain: $A_{vo} = 1 + R_2/R_1$



Voltage follower/Buffer circuits

The lowest gain that can be obtained from a non-inverting amplifier with feedback is 1. When the non-inverting amplifier gives unity gain, it is called voltage follower because the output voltage is equal to the input voltage and in phase with the input voltage. In other words the output voltage follows the input voltage.

$v_{out} = Av_d = A\ (v_1 ? v_2)$

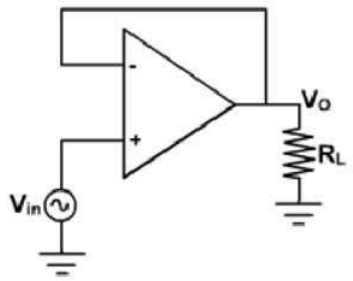
$v_1 = v_{in}$

$v_2 = v_{out}$

$v_1 = v_2$ if $A >> 1$

$v_{out} = v_{in}$.

The gain of the feedback circuit (B) is 1.



Module VI: Application of Operational amplifiers:

Op-Amp as Adder

A basic summing amplifier circuit with three input signals is shown on Figure 1.

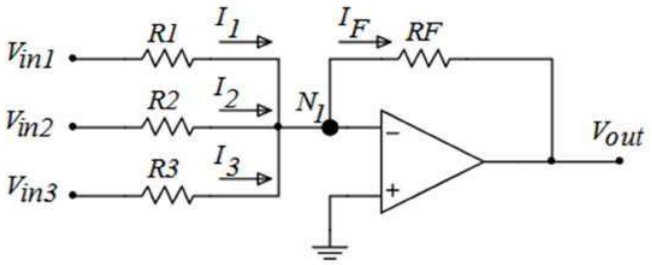


Figure 1. Summing amplifier

Current conservation at node N_1 gives

$$I_1 + I_2 + I_3 = I_F \qquad (1.1)$$

By relating the currents I_1, I_2 and I_3 to their corresponding voltage and resistance by Ohm's law and noting that the voltage at node N_1 is zero (ideal op-amp rule) Equation (1.1) becomes

$$\frac{V_{in1}}{R1}+\frac{V_{in2}}{R2}+\frac{V_{in3}}{R3}=-\frac{V_{out}}{RF} \qquad (1.2)$$

And so V_{out} is

$$V_{out}=-\left(\frac{RF}{R1}V_{in1}+\frac{RF}{R2}V_{in2}+\frac{RF}{R2}V_{in3}\right) \qquad (1.3)$$

The output voltage V_{out} is a sum of the input voltages with weighting factors given by the values of the resistors. If the input resistors are equal $R1=R2=R3=R$, Equation (1.3) becomes

$$V_{out}=-\frac{RF}{R}\left(V_{in1}+V_{in2}+V_{in3}\right) \qquad (1.4)$$

The output voltage is thus the sum of the input voltages with a multiplication constant given by $\frac{RF}{R}$. The value of the multiplication constant may be varied over a wide range and for the special case when $RF = R$ the output voltage is the sum of the inputs

$$V_{out}=-\left(V_{in1}+V_{in2}+V_{in3}\right) \qquad (1.5)$$

The input resistance seen by each source connected to the summing amplifier is the corresponding series resistance connected to the source. Therefore, the sources do not interact with each other.

OP-Amp as Subtractor:

This fundamental op amp circuit, shown on Figure 2, amplifies the difference between the input signals. The subtracting feature is evident from the circuit configuration which shows that one input signal is applied to the inverting terminal and the other to the non-inverting terminal.

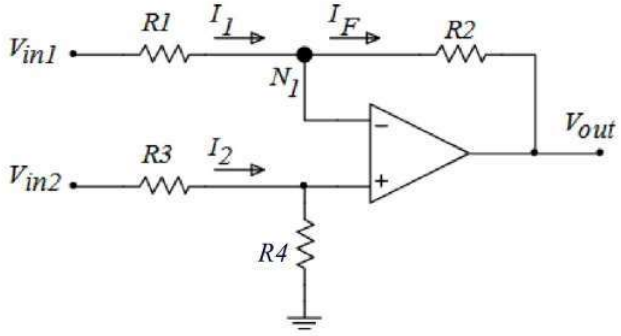


Figure 2. DNerence A mplifter

Before we proceed with the analysis of the dilTerence amplifier let's think about the overall behavior of the circuit Our goal is to obtain the ditTerence of the two input signals (Up_2 - Up;). Our system is linear and so we may apply superposition in order to find the resulting output. We are almost there once we notice that the contribution of the signal U,,,r to the ouQut is

$$V_{out2} = V_{in2}\left(\frac{R4}{R3+P4}\right)\left(1-|-\frac{R2}{P1}\right) \qquad (t.6)$$

and the contribution of signal Kp, is

$$V_{out1} = -V_{in1}\left(R2\right) \qquad (1.7)$$

And the ouQut voltage is

$$V_{out} = V_{out2} - V_{out1} = V_{in2}\left(\frac{R4}{R3+R4}\right)\left(1+\frac{R2}{R1}\right) - V_{in1}\,\frac{R2}{R1} \qquad (<*)$$

Note that in order to have a subtracting circuit which gives —*0* for equal inputs, the weight of each signal must be the same. Therefore

$$\left(\frac{/t4}{+/t4}\right)\left(+\frac{A2}{III}\right)\frac{/t2}{it}\ A3 \qquad (1.9)$$

which holds only if

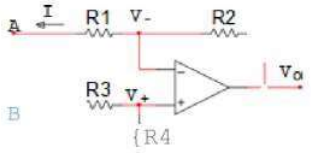
$$P4 \quad A2 \qquad (1.10)$$

The ouQut voltage is now

$$V_{out} = \frac{R2}{R1}(V_{in2} - V_{in1}) \qquad (;;;)$$

which is a difference amplifier with a differential gain of R2/Rf and with zero gain for the common mode signal. It is often practical to select resistors such as *R4—R2* and *R3 —RI.*

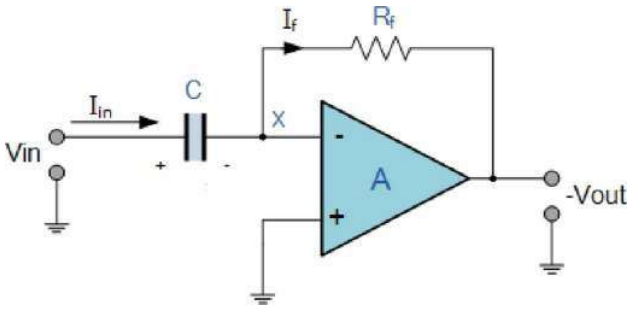
The fundamental problem of this circuit is that the input resistance seen by the two sources is not balanced. The input resistance between the input terminals A and B, the differential inpul resistance, (see Figure 3) is -



jure 5. D0ferentin I amplifier

Since P+ = U_ , Ug = RI Z + fi3 Z and thus Qg = 2fi1 . The desire to have large input resistance for the ditTerenual amplifier is the main drawback for this circuit This problem is addressed by the insbumentation amplifier dismissed next.

Op-amp Differentiator Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (Rf/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op—amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first—order effect, which determines the frequency response of the op—amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R{.

Ok, some math's to explain what's going on!. Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as.

$$I_{IN} \quad I_F \text{ and } \quad I_F = \frac{\quad}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = CCVI$$

rhe rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV}{dt}$$

ut dQ/dt is the capacitor current,i

$$I = C\frac{dV_{IN}}{dt} = I_F$$

$$-\frac{V_{OUT}}{R_F} = C\frac{dV}{dt}$$

rom which we have an ideal voltage output for the op—amp differentiator is given as:

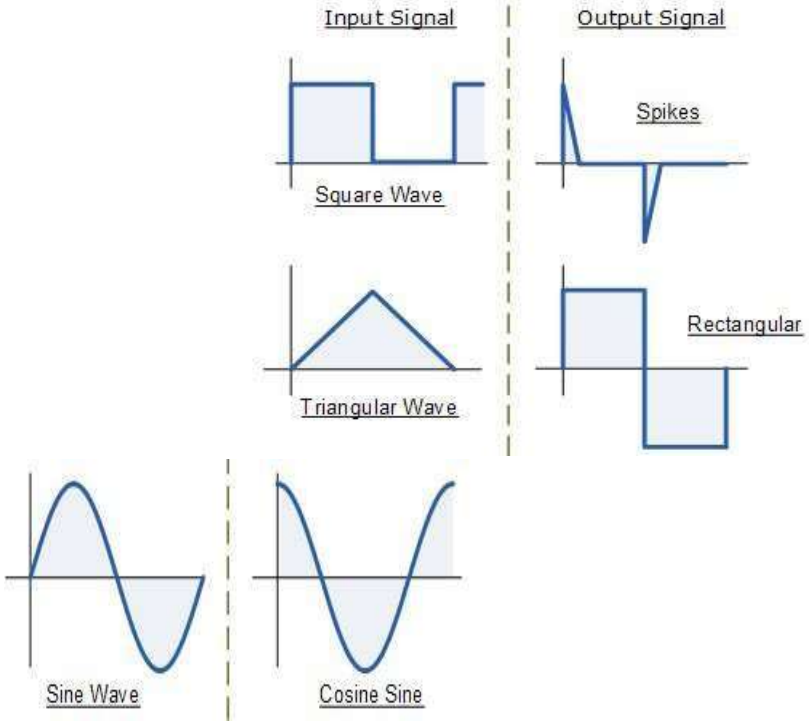
$$V_{OUT} \quad -R_F C\frac{dVg,}{dt}$$

Therefore, the output voltage Vout is a constant times the derivative of the input voltage Vin with respect to time. The minus sign indicates a 1800 phase shift because the input signal is connected to the inverting input terminal of the operational amp1if:er.

One final point to mention, the Op-amp Differentiator circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed—loop stability is required.

Op-amp Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.

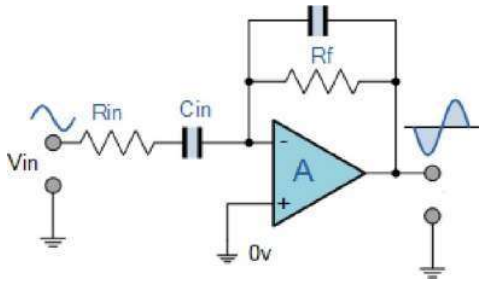


Limitation of differentiator circuit and its solution

One final point to mention, the Op—amp Differentiator circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itsek. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed—loop stability is required.

Improved Op-amp Differentiator Amplifier

Rf



Cf

A (dB)

Rn

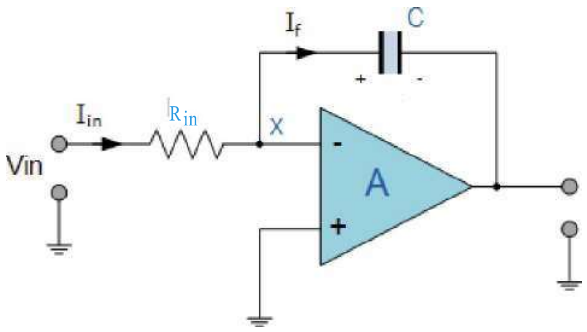
-20dB/decade

C in Rf

Cf Rin

Adding the input resistor Rin limits the differentiators increase in gain at a ratio of R{/Rin. The circuit now acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies giving much better noise rejection. Additional attenuation of higher frequencies is accomplished by connecting a capacitor CQ in parallel with the differentiator feedback resistor, RQ. This then forms the basis of a Active High Pass Filter as we have seen before in the filters section.

Op-amp Integrator Circuit



As its name implies, the Op—amp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration, that is we can cause the output to respond to changes in the input voltage over time as the op—amp integrator produces an output voltage Mick is proportional to the integral oZthe input ve/rage.

In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

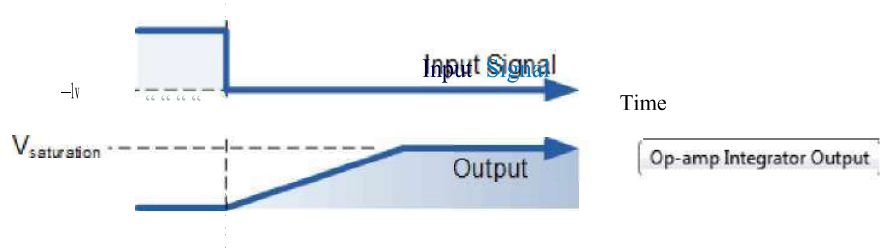
When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the unchanged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of Xc/Rin is also very small giving an overall voltage gain of less than one, (voltage follower circuit).

As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, (‹) of the series RC network. l4egative feedback forces the op—amp to produce an output voltage that maintains a virtual earth at the op—amp's inverting input.

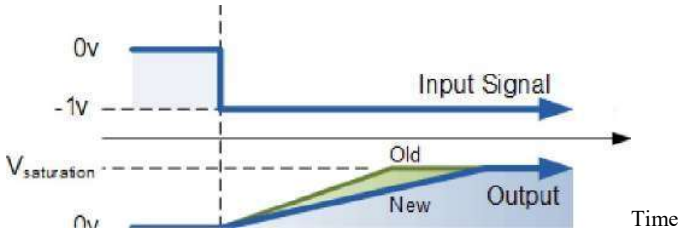
Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op—amp's output (which is negative), the potential voltage, Ve developed

across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor (Xc/Rin) is now infinite resulting in infinite gain. The result of this high gain (similar to the op—amps open—loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

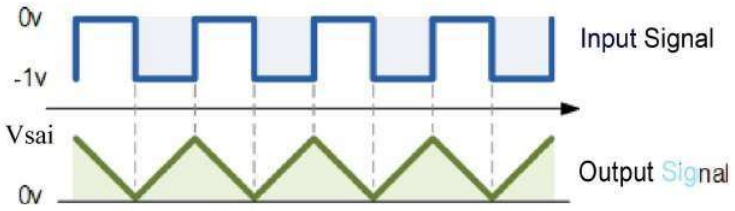


The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed for example.



If we apply a constantly changing input signal such as a square wave to the input of an IntegmtorArnpHfmthenthecapacitorwihchargeanddiihargein esponseto changesmtheinputsign#.ThisrestJtsUttheoutputsign#beingthatofasawtooth waveformwhoseoutputisaffectedbytheRCtUneconstantoftheresistor/ CltO combinationbecauseathigherfrequencies,thecapacitorhaslesstirnetofuflycharge. This type of circuit is also known as a Ramp Generator and the transfer function is given

Op-amp Integrator Ramp Generator



We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacito£ divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout the£efore: —Vout = Q/C. If the capacito£ IS CJ£ff Q and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c - \frac{Q}{C}, \qquad V_c = V_x - V_{out} \qquad 0 \qquad V_{out}$$

$$\frac{dV_{out}}{dt} \quad " \quad \frac{dQ}{Cdt} \quad " \quad \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its mveminginputtenninMiszero,X=o,theinputcu entl(in)fouñngtluoughtheinput resistor,Rinis venas:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

ltte current flowing through the feedback capacitor C is given as-

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

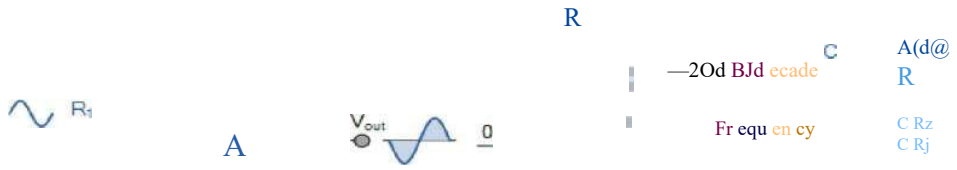
Where $\omega = 2\pi f$ and the output voltage Vout is a constant 1/RC times the integral of the input voltage Vin with respect to time. The minus sign (−) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

Limitation of Intregator circuit and its solution

If we changed the above square wave input signal to that of a sine wave of varying frequency the Op—amp Integrator performs less like an integrator and begins to behave more like an active "Low Pass Filter", passing low frequency signals while attenuating the high frequencies.

At oflz or DC, the capacitor acts like an open circuit blocking any feedback voltage resulting in very little negative feedback from the output back to the input of the amplifier. Then with just the feedback capacitor, C, the amplifier effectively is connected as a normal open—loop amplifier which has very high open—loop gain resulting in the output voltage saturating.

This circuit connects a high value resistance in parallel with a continuously charging and discharging capacitor. The addition of this feedback resistor, R2 across the capacitor, C gives the circuit the characteristics of an inverting amplifier with finite closed-loop gain of RTR,. The result is at very low frequencies the circuit acts as an standard integrator, while at higher frequencies the capacitor shorts out the feedback resistor, R2 due to the effects of capacitive reactance reducing the amplifiers gain. the AC •• P-arn P I Ucejgralor wich DC Gain Control



UnWke£heDCinte atorarnpHfierabovewhoseoutputvoltagea£anyinstan£wiflbethe inte a1ofawaveforrnsothatwhentheinputisasquarewave,theou£putwavetorrn will be triangular. For an AC integrator, a sinusoidal input wavefo xm will produce another sine wave as its output which will be 9o° out—of—phase urirh rhe input producing a cosine wave.

Further more, when the input is triangular, the output waveform is also sinusoidal. This then toxmsthe basis of a Active LowPass Filtex as seen before in the filters section tutorials with a corner frequency given as.

Instrumentation Amplifier

Figure 4 shnws our modified differential amplifier called &e instrumentation amplifier (lA). Op amps UI and W act as voltage followers for the signals Hai and U which see the infinde input resistance ofop amps NJ and W. Assuming ideal op amps, the voltage

at the inverting terminals of op amps U2 and U are equal to theé corresponding input voltages The resulting current flowing through resistor *RI* is

$$I_1 = \frac{V_{in1} - V_{in2}}{R1} \tag{1.12}$$

Since no current nows into the terminals of the op amp, the current flowing through resistor R2 is also given by Equation (1.12).

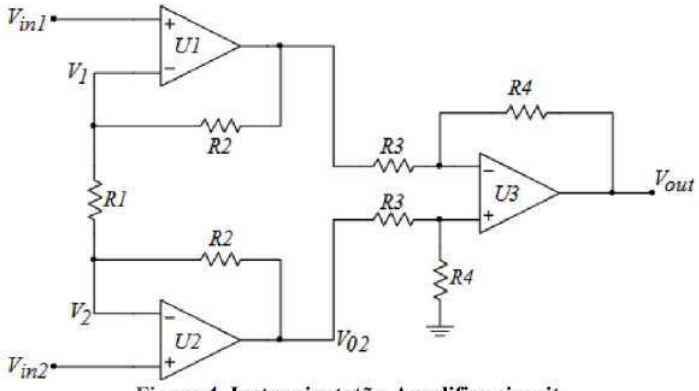


Figure 4. Instruuientatñn Amplifier circuit

Since our system is linear the voltage at the output of op-amp *UI* and op-amp W is given by superposition as

$$V_0' = \left(1 + \frac{R2}{R1}\right)V_{in1} - \frac{R2}{R1}V_{in2} \tag{1.13}$$

$$V_{02} = \left(1 + \frac{R2}{R1}\right)V_{in2} - \frac{R2}{R1}V_{in1} \tag{1.14}$$

Next we see that op amp *U3* is arranged in the difference amplifier configuration exam tried in the previous section (see Equation (1.11)). The output of the difference amplifier is

$$V_{out} = \frac{R4}{R3}\left(1 + \frac{2R2}{R1}\right)(V_{in2} - V_{in1}) \tag{1.15}$$

The differential gain, $p\frac{}{3} + + \frac{2R21}{R1}\Big)$, may be varied by changing only one resistor: *RI.*

Op-amp Comparator

A comparator. in electronics. is a circuit configuration that compares two voltages (or currentsJ and indicates which one is larger Thus. the inputs to a comparator should be different in nature. Comparators can be easily configured using op-amps. since the op-amps have high gain and balanced drl erence inputs. Theoreticaky. an op-amp in open-loop configuration (no feedback can be used as a comparator. When the input vokage at the non-inverting terminal V. is greater than the voltage at the inverting input terminal Ve. the output the op-amp saturates at its positive extreme. then the non-inverting input voltage drops below the inverting input vokage. the op-amp output switches to its negative saturation feveL Comparator circuits are most widely used in analog-to-digital converters ADCs1 and in oscillators.

Op-amp Inverting Comparator

In an inverting comparator. the input voltage V, is appMed to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to reference voltage. through resistors Rt and Rt. As long as the input voltage Vol is lesser than the reference voltage Vref. the output of the op-amp remains positively saturated then Vo goes above the reference voltage. the output of the op-amp swkches to Its negative saturation level and remains negatively saturated as long as V, is less than Vref The circuit ofa comparator using op-amp ”e shown in the tgure below.

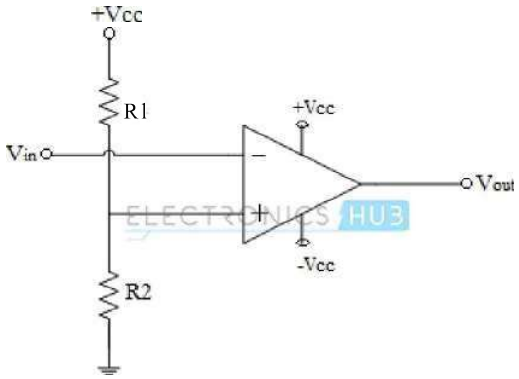


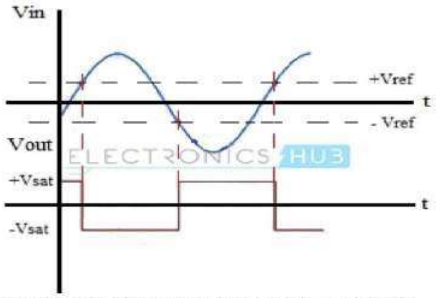
Fig: Ihvertirig Comparator using Op-amp

By choosing the sales of resistors R and Rt. the reference voltage V« f can De adjusted and comparator can De used to compare input voltage with the corresponding reference voltage

$$V_{out} = +V_{sat}: \text{ if } V_{in} < V_{ref}$$

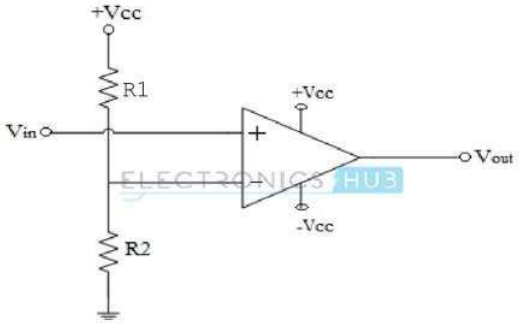
$$= -V_{sat}: \text{ if } V_{in} > V_{ref}$$

The input ance output was eforms of an op-amp inceрting comparator is shown in the figutre DeLow.



Fts : friput Output Vv*av•eforms of Inv•ertirig orriparator

Op-amp Non-Inverting Comparator



diy: hon-ltte-kg Ccrmparator u y Op-amp

In the case of an op-amp non-inverting comparator. the input vol1ape Var applied to the non-inverting input terminal and the reference voltage. Vref. is connected to the inverting input terminal then the input vol1ape Var Greater than the reference voltage Vref- the op-amp output is positively saturates In practice. the difference hon-h ref* ll1be a positive value. Since there is no feedback to the op-amp input. the open-loop pain of the op-amp wik be infinity Hence the output wil1swing to its maximum possible value. +Vsat. then the input vol1ape fal1s below the reference voltage. the output switches to its negative saturation voltage.

$$V_{out} = +V_{sat}: \text{ if } V_{in} > V_{ref}$$

$$= -V_{sat}: \text{ if } V_{in} < V_{ref}$$

Op-amp Logarithmic Amplifier

An operational amplifier can be configured to function as a Logarithmic amplifier. or simply Log amplifier. Log amplifier is a non-linear circuit configuration. where the output is Ntimes the Logarithmic vale of the input vol1age applied. Log amplifiers find the applications in computations such as multiplication and division oT signals. computation of powers and roots. signal compression ana decompression. as well as in process control in industrial appMcations A Log amplifier can be constructecl using a bipolarjunction transistor in the feeaback to the op-amp. since the col1ector current of a BJT is togarithmically related to its base-emitter vol1age.

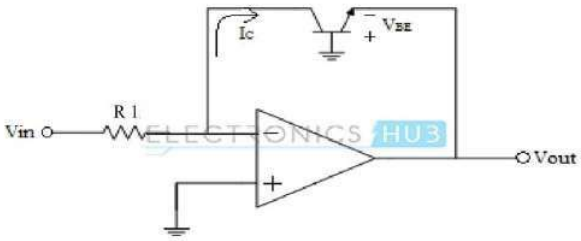


Fig. Op-amp oparilhmic .Mphfier

The circuit ofa fundamental fog ampler using op-amp is shown in the fgure above The necessary condition of the fog ampler to work is that the input voltage always must be positive It can be seen that V t — V

Since the collector terminal of the transistor is held at virtual ground and the base terminal is also grounded. the voltage-current relationship becomes that ofa diode and is given by.

$$I_E = I_f.[e^{/kT} - 1]$$

there.

Iy - the saturation current.

k - Bokzmann's constant

T - absolute temperature (in0

Since $I_E = I_C$ for grounded base transistor.

$$I_C = I_S.\ [e^{q(Vbe)/kT} - 1]$$

$$(I_C/I_S) = [e^{q(Vbe)/kT} - 1]$$

$$(I_C/I_S) + 1 = [e^{q(Vbe)/kT}]$$

$$(I_C+I_S)/I_S = e^{q(Vbe)/kT}$$

$$e^{q(Vbe)/kT} = (I_C/I_S) \text{ since } I_C >> I_S$$

Taking natural log on both sides of the above equation, we get

Vp - (kT/q\ milk/IU

The collector current I¿' Vin' R and Vout' —V

Therefore,

$$V_{out} = -(kT/q) \ln[V_{in}/R_1.I_S]$$

The output of the circuit is, thus, proportional to the log of the input voltage. However, the output is dependent on the saturation current which varies from transistor to transistor and also with temperature. Compensation circuits can be added to stabilize the output against these variations.

Anti-Logarithmic Amplifier or Exponential Amplifier

Anti-logarithmic or exponential amplifier (or simply antitog amplJfierJ is an op-amp circuit confguration. whose output is proportional to the exponential value or anti-Log value of the input Antitog amplifier does the exact opposite of a Log amplifier. AntiLog amplifiers along with log amplifiers are used to perform analogue computations on the input signals The circuit of an antiLog amplifier using op-amp is shown in the figure below

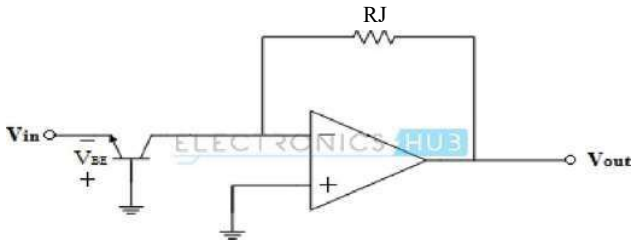


Fig: .Qtr-logarithmic .Mplifier

It is noted that by exchanging the positions of the transistor and the resistor. the Log amplifier can be made to work as antiLog amplifier. The base-cokector vol1age of the transistor is maintained at grouna potentiaL from the virtual ground concept. The curre•! !E for the transistor is given by.

$$I_E = I_S.[e^{q(Vbe)/kT} - 1]$$

For a grounded base transistor. !E' !C Therefore.

$$I_C = I_S.[e^{q(Vbe)/kT} - 1]$$

Where. Iq - saturation current of the transistor.

C out - Ic R§

$$V_{out} = I_S.[e^{q(Vbe)/kT} - 1].R_1$$

Also. for the above circuit Vo - —V Therefore.

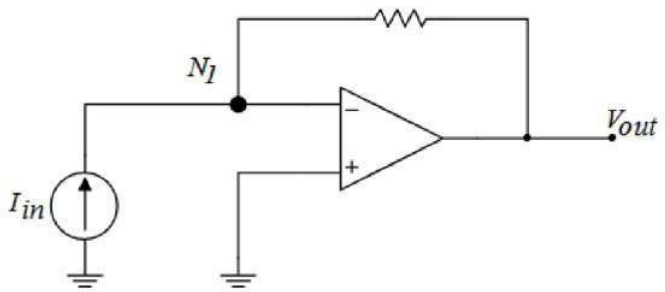
$$\mathbf{V_{out} = R_1.I_S.[e^{q(-V_{in})/kT} - 1]}$$

Antitog amplers also surer from unstable outputs. due to the variations in Iy for different transistors and temperature dependence Compensating circuits can be added to stabilize the output against such variations

C urrenl to voltage converters

A variety of transducers produce electrical current in response to an environmental condition. Photodiodes and photomultipliers are such transducers which respond to electromagnetic radiation at various frequencies ranging from the infrared to visible to y-rays.

A current to voltage converter is an op amp circuit which accepts an input current and gives an output voltage that is proportional to the input current. The basic current to voltage converter is shown on Figure S. This circuit arrangement is also called the *transresistance amplifier.*



Current tn vnttnge buoy erter

/p represents the current generated by a certain transducer. If we assum e that the op amp is ideal, KCL at node NJ gives

$$I_1 + \left(\frac{V_{out} - 0}{R}\right) = 0 \Rightarrow \boxed{V_{out} = -RI_1} \qquad (1.16)$$

The "gain" of this amplifier is giveo by R. This gain is also c:alled the see sitivity of the converter. Note that if high sensitivity is required for example lV/pV then the resistance R should be 1 Mif2. For higher sensitivities unrealistically large resistances are required.

A current to voltage converter with high sensitivity may be constructed by employing the T feedback network topology shown on Figure 6.

In this case the relationship between Uo2Jf and Zz is

(— —)

Voltage to C urre nt converter

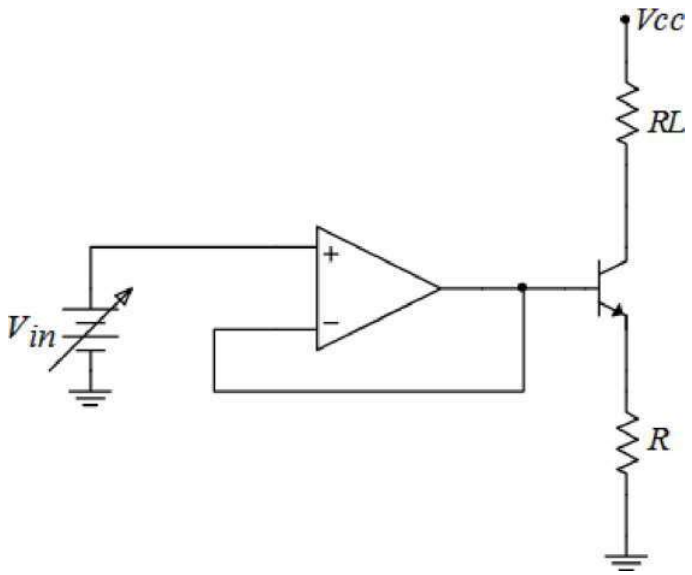
A voltage to current (V-I) converter accepts as an input a voltage Vin and gives an output current of a certain value.

In general the relationship between the input voltage and the output current is

$$I_{out} = SV_{in} \qquad \text{(i.ia)}$$

Where S is the sensiuvity or gain of the V-I converter.

Figure 7 shows a voltage to current converter using an op-amp and a transistor. The op- amp forces its positive and negative inputs to be equal; hence, the voltage at the negauve input of the op-amp is equal to km. The current through the load resistor, RL, the transistor and R is consequently equal to K fi. We put a transistor at the output of the op-amp since the transistor is a high current gain stage (often a typical op-amp has a fairly small output current limit).



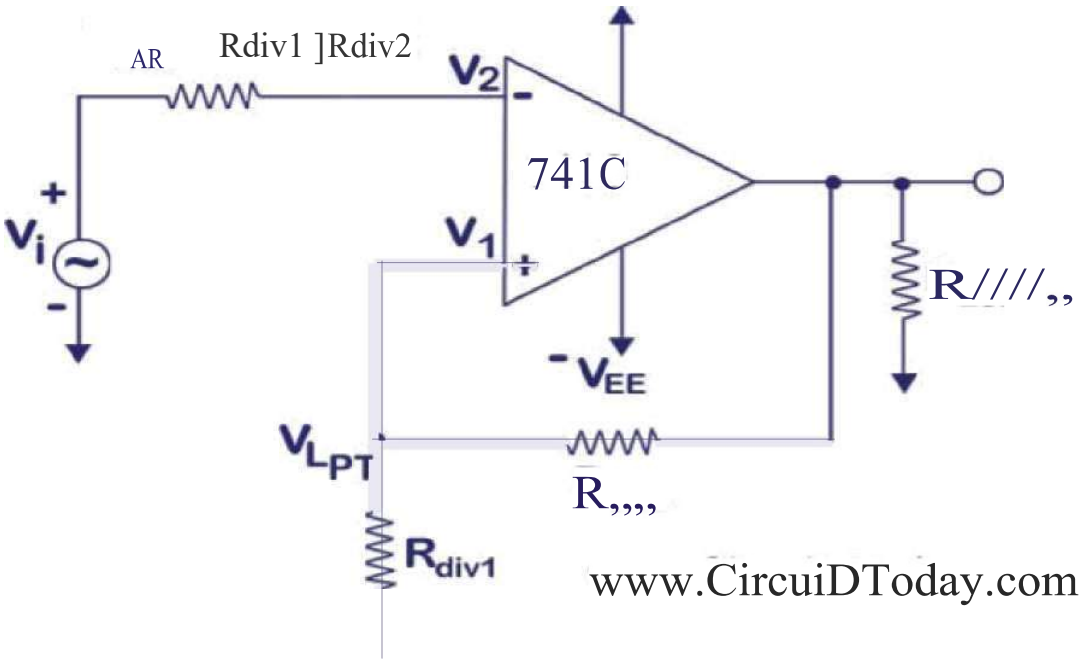
1'n¥age tn current converter

SCHMITT TRIGGER USING OP-AMP

Schmitt Trigger or Regeneratiw Comparator Circuit

A Schmitt trigger circuit is also called a regenerative comparatcr circuit The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use ofa regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise vokages. Shown below is the circuit diagram of a Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or puke. Thus, it can also be called a squaring circuit

SCHMITT TRICGER USING OP - AMP 741IC



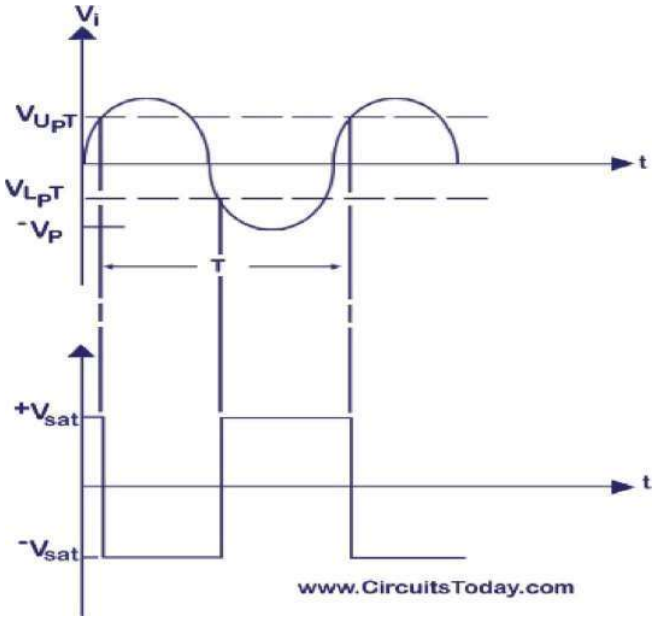
Schmid Trigger Circu°e Using Op-Amp uA74l IC

As shown in the circuit diagram, a voltage divi‹)er with resisixrs Rdivl and Rdiv2 is set in the positive feedback of the 741 IC cp-amp. The same values of Rdivl and Rdiv2 are used to get the resistance value Rpar = Rdivl ||Rdiv2 which is connected in series with the input voltage. Rpar is used to minimize the otTset problems. The vohage across RI is fedback to the non-inverting input.

The input voltage Vi triggers m changes the state of output Vout every time it exceeds its voltage levels above a certain threshold value called Upper Threshold Voltage (Vupt) and Lower Threshold Voltage (Vlpt).

Let us assume that the inverting input vokage has a slight positive value. This will cause a negative value in the output This negative voltage is fedback to the non-inverting terminal (+) of the op-amp thmugh the vokage divider. Thus, the value of the negative voltage that is fedback to the positive terminal becomes higher. The value of the negative voka e becomes again higher until the circuit is driven into negative satumtion (-Vsat). Now, let us assume that the inverting input voltage has a slight negative value. This will cause a positive value in the ouQut. This positive voltage is fedback to the non-inverting terminal (+) of the Citi-amp through the voltage divider. Thus, the value of the positive voltage that is fedback to the positive terminal becomes higher. The value of the positne vokage becomes again higher until the circuit is driven into positive saturation (+Vsat). This is why the circuit is also named a re nerative comparator circuit.

acH u lv vo lac er‹ - If'dPUT Af'd O O lJTPUT UVAWS ••O •'tE



When Vout = -1-Vsat, the va hage across Rdivl is called Upper Thresbo kl Voltage (Vupt). The input vahage, Vin must be tightly more positive than Vupt ioorder to cause the output Ve to switch fiom +Vsat to -Vsat. When the ipput voltage is less than Vupt, the output voltage Vout is at -1-Vsat.

Upper Threshold V‹dtage, Vup4 = +Vsa4 {Rdivl/}RdivI+Rdiv2])

When Vout = -Vsat, the voltage across Rdivl is called Lawer Thresfio kl Voltage (Vipt). The ipput vahagg Vin must be tightly mare negaitive than Vipt reorder to cause the output Ve to switch fiom -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat.

If the value of Vupt aixl Vipt are higher than the input ooise voltage, the positive feedback will eliminate the false output transitions. Wdh the help of positive feedhack aixl its regenerative behaviour the output voltage will swdch Gael between the positive aixl negahve saturation voltages.

Hysteresis Charac&#stics

Since a compaiator circud with a positive feedba‹& is used, a dead band coixldion hysteresis can occur in the output. When the input of the comparator has a value higher than Vupt, its output switches fiom +Vsat to -Vsat aixl reverts ba‹& to its original state, +Vsat, when the input value goes below Vipt. This is shown in the figure below. The hysteresis va hage can be cakulated as the difference between the upper aixl lower threshold valtagez

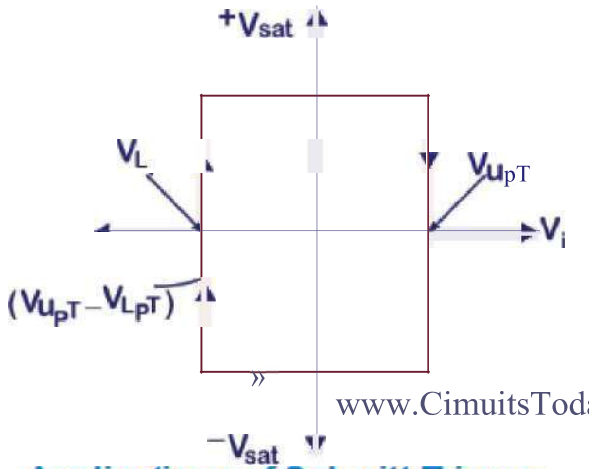
Vhysteresis = Vupt — Vlpt

Subsitutipg the values of Vupt and Vipt fiom the above equations.

Vhysteresis = +Vsat (Rdiv1fRdiv1+Rdiv2) — {- Vsat (Rdivl/Rdiv1+Rdiv2)}

vntu«e ñ = ;eaivi/ndivi+edi<) t+vat —t-v t)j

SCHMITT TRIOOER - INPUT OUTPUT CHARECTERIBTICS•
HYSTERISfS VOLTAGE PLOT



Applications of Schmitt Trigger

Schmitt trigger is mostly used to convert a very slowly varying input voltage into an output having abruptly varying waveform occurring precisely at certain predetermined value of input voltage. Schmitt trigger may be used for all applications for which a general comparator is used. Any type of input voltage can be converted into its corresponding square signal wave. The only condition is that the input signal must have large enough excursion to carry the input voltage beyond the limits of the hysteresis range. The amplitude of the square wave is independent of the peak-to-peak value of the input waveform.

Precision Rectifier

Precision half-wave rectifiers

An operational amplifier can be used to linearize a non-linear function such as the transfer function of a semiconductor diode. The classic half-wave rectifier circuit shown in Figure 1 exhibits considerable distortion and truncation when the input signal level is low.

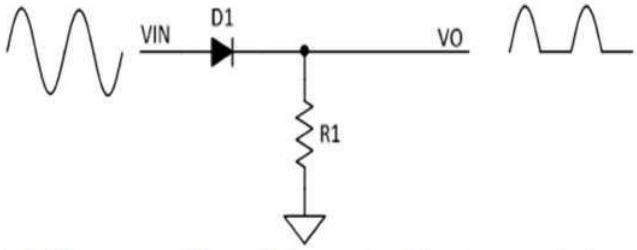


Figure 1: Simple half-wave rectifier with large signal input to minimize output distortion

If the diode is placed in the feedback of an operational amplifier the linearity at small signal levels is greatly improved as a result of the high amplifier gain. At high signal levels the circuit functions practically as if perfect. Signals at low frequencies down to a few millivolts peak will be accurately half-wave rectified. The only limit is the open loop gain and slew rate of the operational amplifier at the highest significant harmonic of the half-wave signal. Higher gain leads to more accurate rectification.

Figure 2 illustrates the classic precision half-wave rectifier. Series capacitor, C_1, blocks DC from the circuit and R_1 provides a path for bias current to operational amplifier, U_1. Diode, D_1, conducts when Vp is positive and unity-gain amplifier, Uz, buffers the rectified signal. Diode, , is reversed biased and therefore not part of the circuit when the input signal is positive. Feedback from Uz applied to the inverting input of Ui. The action of the output of Ui é to go to such a voltage that the signal at the inverting input matches the signal at the non-inverting inpuL Thus, since Di is in the long feedback loop of Ui, the output of Uz matches Vp during the time that Vp is positive — i.e. output waveform matches input waveform even when Vp is only in the low millivok range.

When Vp is negative then the output of Ui is negative and Di is reversed biased — thus the non-inverting input to U2 is zero and Vo is zero. Diode, , is now forward biased and again the output of Ui goes to the required voltage so that its inverting input matches its non-inverting input. During this time there is a voltage drop across Rs since V is zero and the inverting input to Ui is negative.

The waveform at the output of Ui requires a very high slew rate as the output transitions from forward bias on one diode to forward bias on the other diode — note the rapid jumps in voltage at the zero crossings. When the amplifier is not capable of slewing fast enough then the leading edge of the half-cycle is truncated. A common error in using this circuit is overlooking the bandwidth requirement of the amplifiers. As a rough guide the gain-bandwidth product of the amplifier should be at least 100 times the frequency of the sine wave or noticeable waveform distortion will occur particularly for low amplitude input signals. With ordinary operational amplifiers the circuits shown here operate up to a few kHz and a few tens of kHz with wider bandwidth amplifiers. Accurate higher frequency operation requires advanced methods beyond the scope of this note.

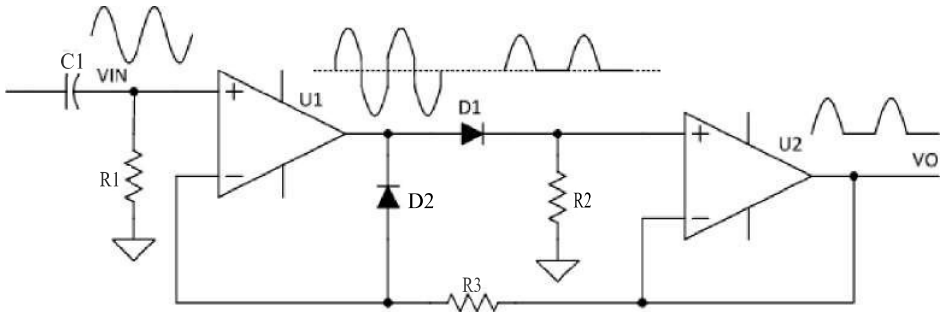


Figure 2 : Precision half-wave rectifier

An alternate form of the precision half-wave rectifier is shown in Figure 3. Ui is an inverting amplifier so the V output of Ut is the negative portion of Vp. Dt conducts when V is negative thus mak ing a positive voltage across Rz which is buttered by Uz- Diode, , provides a feedback path when Vp is positive.

An alternate form of the precision half-wave rectifier is shown in Figure 3. Ui is an inverting amplifier so the Vo output of Uz is the negative portion of V . Di conducts when Vp is negative thus making a positive voltage across Ri which is bulTered by Ui. Diode, , provides a feedback path when V is positive.

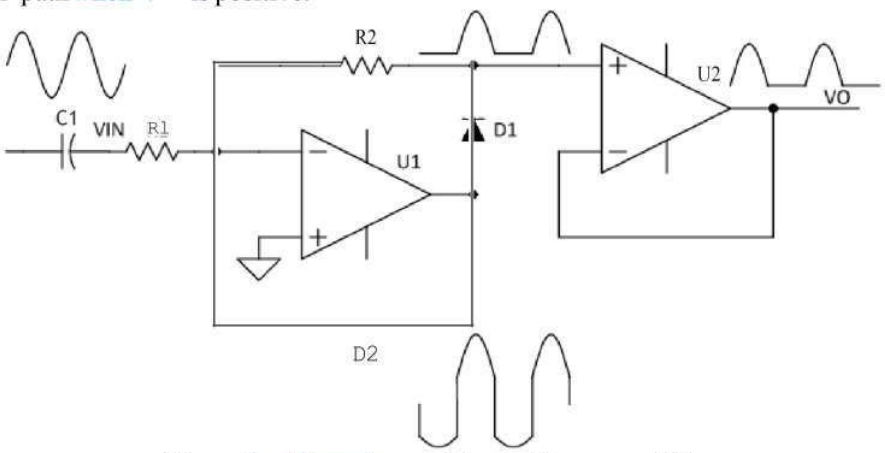


Figure 3 : Alternate precision half-wave rectifier

Figure 4 shows a modified version of the circu it in Figure 3 to provide smooth the half-wave rectified signal into a steady DC voltage. Circuits like this are known as "average responding" and are often used in low-cost non-true-rms responding AC voltmeters. Average responding detectors are generally calibrated to produce a voltage corresponding to the rms of a sine wave and will be inaccurate for any other waveform. The average value of the mctified signal is across Ct. For a sine wave the half-wave DC average voltage is given by Equation 1. This

equation is on ly hue for sine waves. Square wave, triangle waves, and other waveforms have different factors. The time constant of R Ct should generally be several hundred milliseconds.

$$V_{DC} = \frac{V_P}{\pi} = V_{rms}\frac{\sqrt{2}}{\pi} = 0.450V_{rms}$$

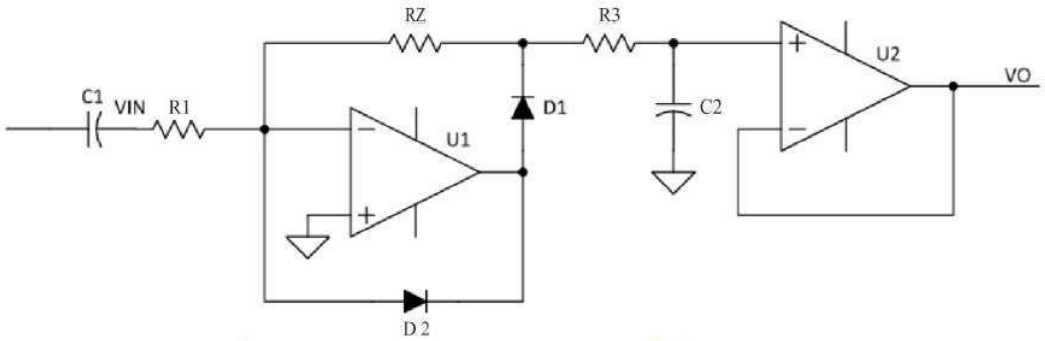


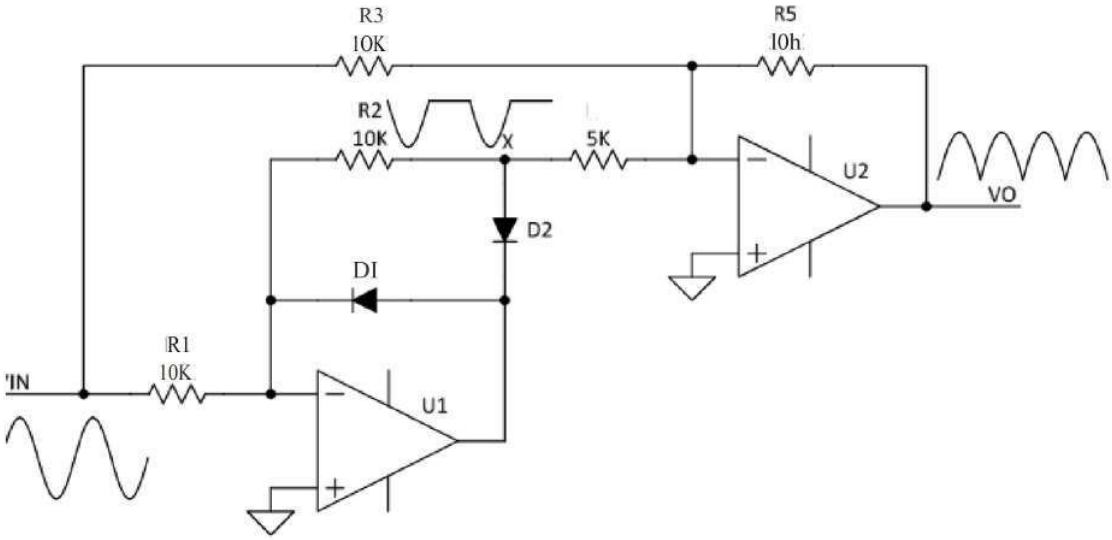
Figure 4: Precision half-wave rectifier with DC smoothing filter.

Precision full-wave rectifiers

A useful signal processing function is the absolute value c uit. The name, full-wave rectifier, is a special case application where the input signal is AC coupled to remove any DC component. That is the only distinction between the two names — the circuits are the same. The more general absolute value circuit operates from DC up to its maximum frequency and is not thought of as a rectifier although it will obviously perform that task.

The classic absolute value circuit is shown in Figure S. Although the circuit might look complicated the analysis is simple when broken into its parts. The circuit around U is just like that in Figure 3 except that the diodes are reversed so the voltage waveform at point X is inverted. Ut and resistors, R , , and R, is an inverting summer with a gain of -1 to Vp and a gain of -2 to the voltage at point X. Note that when Vp is negative the voltage at point X is zero, as D2 reversed biased and D; is forward biased. In that case the output voltage of U2. V , is the inverted magnitude of Vp — the voltage at point X is zero and contributes nothing. When Vp is positive the voltage at point X is the negative of Vp. The output of U_S then the negative of V minus twice the negative of V since the gain of U_S to the voltage at point X is -R /Rt which is -2. Expressed as an equation, Up = —Ptp — (—2)K,p = Utp.

For proper operation all the resistors should be matched and the 5K should be very accurately half the 10K. Otherwise there will be waveform distortions and there will be considerable error for operation at low voltages in the tens of millivolts and less.



Figum 5: Classic absolute value circuit

An absolute value circuit based on a dual half-wave circuit is shown in Figure 6. Analysis of the circuit is simple although a common error is omitting the effect of R . For this circuit to work properly it is important that R_S and R be matched in resistance and that and R, be matched as well. Ideally all four resistors match. Rt just sets a scale factor and can be higher or lower than the other resistors as shown in a subsequent example. The analysis will be performed with all five resistors the identical value as shown in the figure. Operation is as follows.

When Vp is positive the output of Ut goes negative so that the voltage at the anode of D_o ,* —Vp and the voltage at the cathode ofD is zero. Thus, Ut acts as an inverting amplifier and V = V

When Vy is negative the output of Ut goes positive so that the voltage at the cathode of D goes positive — an error is to assume it goes to —Vp — keep in mind the path through R3. Let us call that voltage V_{X-} We note that the voltage at the inverting input of Ut must ako be V_{X-} We then note that the total feedback current to the inverting input of Ut is // = Up/ R_2 + Pp/ (R_3 -1- *R*)— (3/2)(U2/10K). Since this current is identical to U,p/10K then Up = —(2/3) *PIN* The non-inverting gain of Ut is 1.5 (remember that R3 is in the circuit) so V = -Vp, a positive voltage.

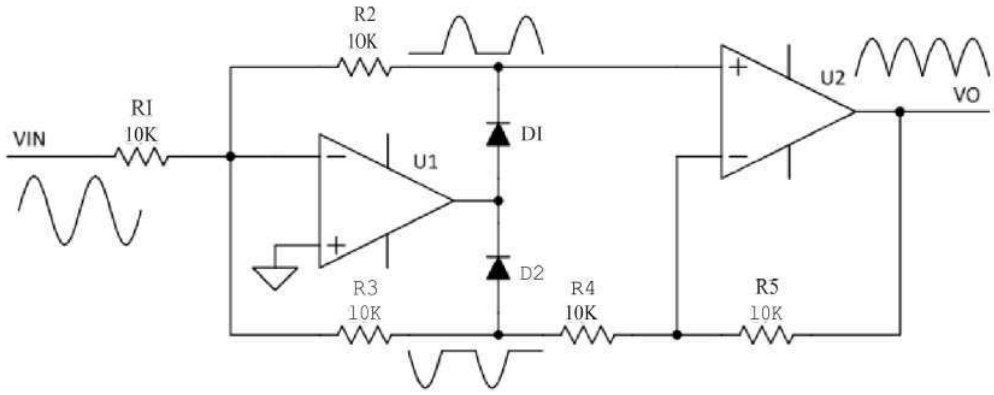


Figure 6: Alternate absolute value circuit

One undesirable trait of the circuits in Figures 5 and 6 is that considerable resistor matching is required for proper operation. Mismatching of the resistors results in a variety of distortions as shown in Figure 7. In the first case the gain is different for the two half-cycles. In the second and third cases the crossover points do not lineup in addition of gain mismatch.

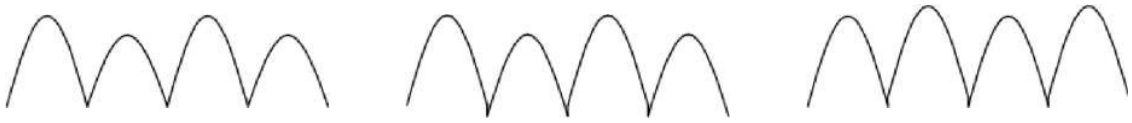


Figure 7: Examples of distortion caused by resistors not being matched

The circuit shown in Figure 8 is believed to be the simplest possible absolute value circu it and has the feature that only two resistors, R;, and Rs. need to be matched. R is nominally the same resistance but does not need to match.

When V is positive Do is forward biased (Dt is reversed biased) and U2 acts as a unity gain buffer to V . Feedback through R; and R2 Ut causes V to match V . When V is negative then D; is forward biased W2 is reversed biased) and the output of Ut goes to the required voltage so that its inverting input matches Vp. U2 is now an inverting amplifier so that V is — V — i.e. always positive.

large, there will be errors at h igh frequencies. The correct amount of capacitance is as small as possible consistent with no oscillation on the V waveform.

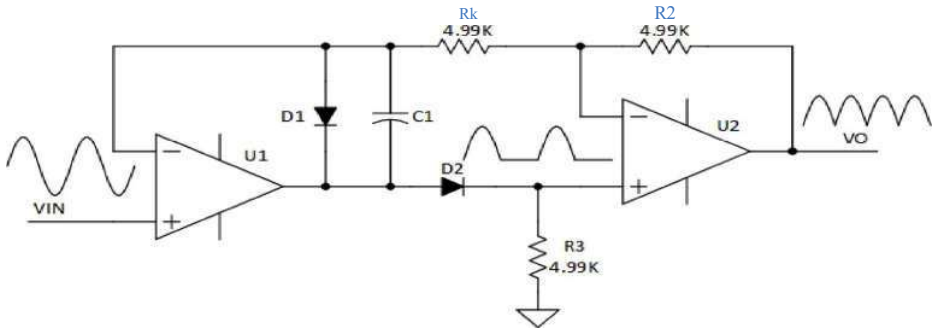


Figure 8 : S implest possible absolute value circuit

Figure 9 shows a precision fu11-wave rectifier with DC smoothing. As shown, V is a DC voltage equal to the rms voltage of V provided that V is a sine wave. That relation will not hold true for other waveforms. The smoothing time constant set by the 33OK and 1 uF capacitors is one-third of a second wh ich gives a full settling time of about 2 seconds. C2 a nd C3 shou ld be smaller to reduce that time. 2) and correspondingly (R,/ R3) shou ld be large as shown to minim ize the effect of stored charge on the smoothing capacitors from affecting operation of Ut .

Ut should have wide bandwidth. Ut and U should be precision DC amplifiers and have very low input bias currents — preferably less than 1 nA.

The voltage across R_2 is a positive half-cycle and the voltage across R_3 is a negative half-cycle. Those half-cycles are DC averaged by filters, R_4C_2 and R_5C_3. The difference amplifier provides a gain a two. With V_{IN} a sine wave of rms voltage, Vrms, the DC output voltage, V_O is found as follows. The two factors of 2 account for the difference amplifier applying a gain of two on the difference between the positive DC average and the negative DC average.

$$V_O = V_{RMS}\left(\frac{2.0}{3.6}\right)\left(\frac{\sqrt{2}}{\pi}\right)(2)(2) = 1.0004V_{RMS} \quad (2)$$

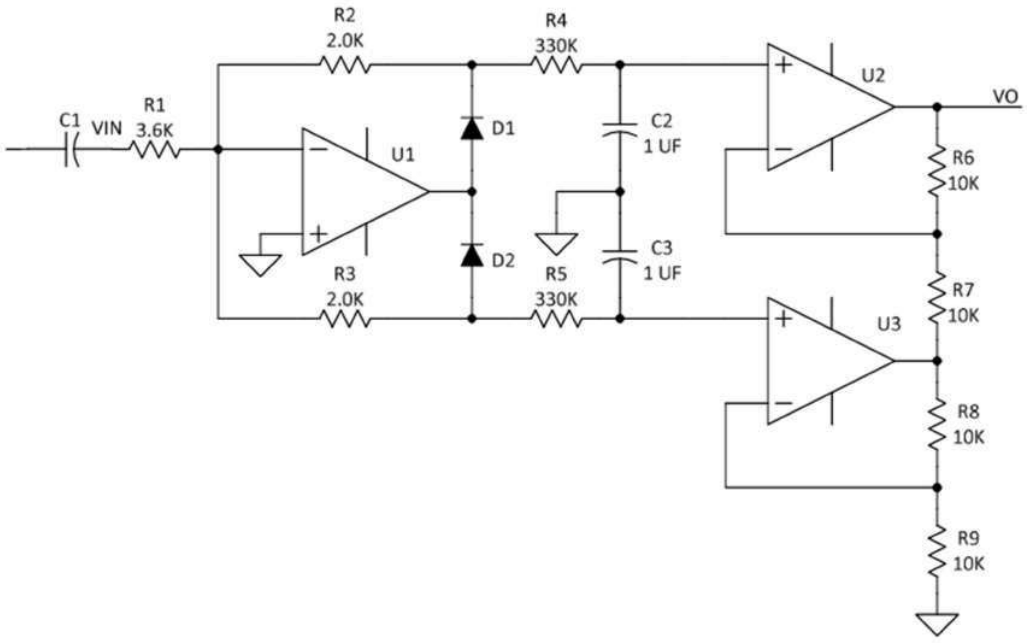


Figure 9: Full-wave rectifier with DC smoothing filter

Module VII: Power amplifiers:

A Power amplifier is large signal amplifier and this is generally a last stage of a multistage amplifier. The function of a practical power amplifier is to amplify a weak signal until sufficient power is achieved to operate a loudspeaker or output device. Typical output power rating of a power amplifier will be 1W or higher. The blocks of a practical amplifier is as follows-Voltage amplifier- Voltage amplifier- Driver stage -Output stage-Speaker. The driver stage operates as a class A power amplifier and supplies the drive for the output stage. The last output stage is essentially a power amplifier and its purpose is to transfer maximum power to the output device (speaker). The output stage generally employ class B amplifiers in push-pull arrangement. A large signal amplifier means much larger portion of load line is used during signal operation compared to small signal amplifier. A small signal amplifier (handle ac signal <10mV) operate over a linear portion of load line. In case of power amplifier, we cannot use small signal approximation directly to calculate voltage gain, current gain and input/output impedance. Ideal power amplifier will deliver 100% of the power it draws from the supply to load. In practice, this can

never occur. The reason for this is the fact that the components in the amplifier will all dissipate some of the power that is being drawn from the supply.

Parameters of power amplifier:

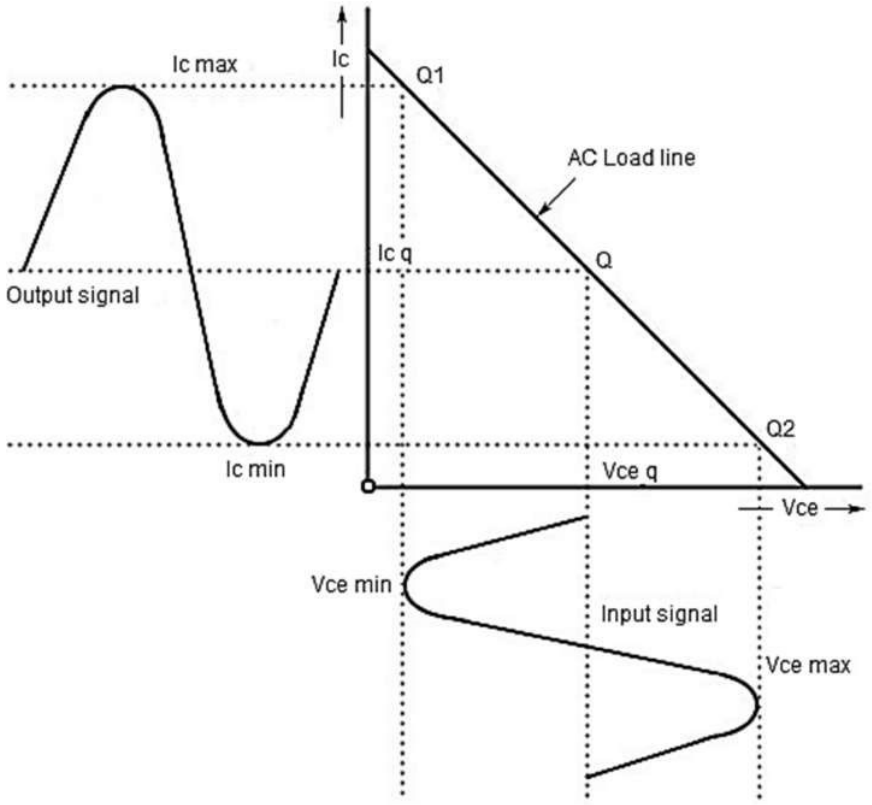
Amplifier Efficiency: A figure of merit for the power amplifier is its efficiency. It is defined as a ratio of output ac power to the input dc power.

Distortion: The change in output wave shape from the input wave shape of an amplifier is known as distortion. The distortion can be reduced using negative feedback in amplifier.

Power dissipation capability: The ability of a power amplifier to dissipate heat is known as power dissipation capability. To achieve better heat dissipation heat sink (metal case) is attached with power transistor. The increase surface area allows heat to escape easily.

Class A power amplifier:

Class A power amplifier is a type of power amplifier where the output transistor is ON full time and the output current flows for the entire cycle of the input wave form. Class A power amplifier is the simplest of all power amplifier configurations. They have high fidelity and are totally immune to crossover distortion. Even though the class A power amplifier have a handful of good feature, they are not the prime choice because of their poor efficiency. Since the active elements (transistors) are forward biased full time, some current will flow through them even though there is no input signal and this is the main reason for the inefficiency. Output characteristics of a Class A power amplifier is shown in the figure below.

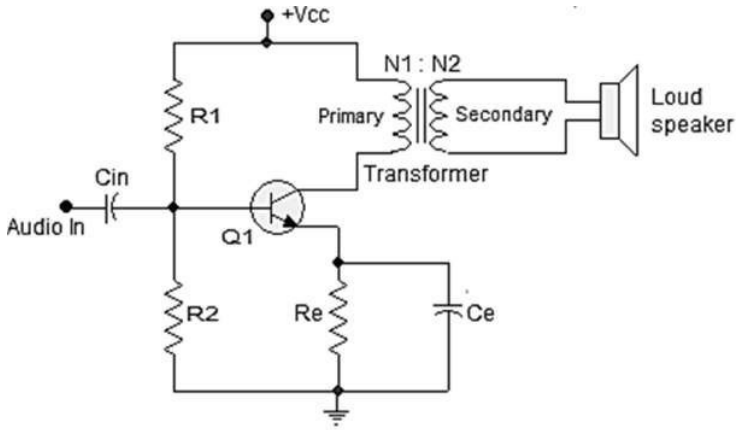


Class A power amplifier output characteristics
AC load line

From the above figure it is clear that the Q-point is placed exactly at the center of the DC load line and the transistor conducts for every point in the input waveform. The theoretical maximum efficiency of a Class A power amplifier is 50%. In practical scenario, with capacitive coupling and inductive loads (loud speakers), the efficiency can come down as low as 25%. This means 75% of power drawn by the amplifier from the supply line is wasted. Majority of the power wasted is lost as heat on the active elements (transistor).As a result, even a moderately powered Class A power amplifier require a large power supply and a large heat sink.

Transformer coupled Class A power amplifier:

An amplifier where the load is coupled to the output using a transformer is called a transformer coupled amplifier. Using transformer coupling the efficiency of the amplifier can be improved to a great extend. The coupling transformer provides good impedance matching between the output and load and it is the main reason behind the improved efficiency. Impedance matching means making the output impedance of the amplifier equal to the input impedance of the load and this is an important criteria for the transfer of maximum power. Circuit diagram of typical single stage Class A amplifier is shown in the circuit diagram below.



Tranformer coupled Class A amplifier

Impedance matching can be attained by selecting the number of turns of the primary so that its net impedance is equal to the transistors output impedance and selecting the number of turns of the secondary so that its net impedance is equal to the loudspeakers input impedance.

Advantages of transformer coupled amplifier:

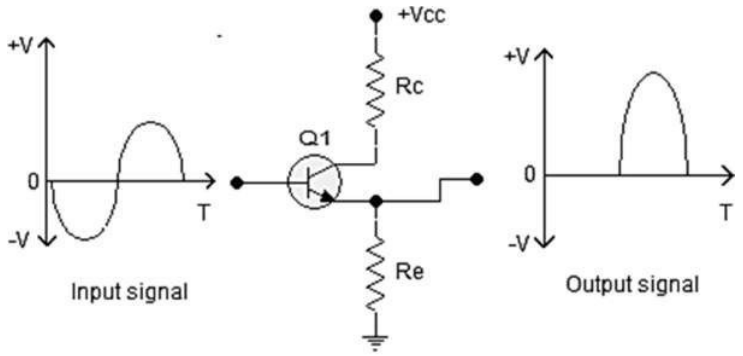
- Main advantage is the improvement of efficiency.
- Provides good DC isolation as there is no physical connection between amplifier output and load. Audio signals pass from one side to other by virtue of induction.

Disadvantages of transformer coupled amplifier:

- It is a bit hard to make/find an exactly matching transformer.
- Transformers are bulky and so it increases the cost and size of the amplifier.
- Transformer winding does not provide any resistance to DC current. If any DC components if present in the amplifier output, it will flow through the primary winding and saturate the core. This will result in reduced transformer action.
- Transformer coupling reduces the low frequency response of the amplifier.
- Transformer coupling induces hum in the output.
- Transformer coupling can be employed only for small loads.

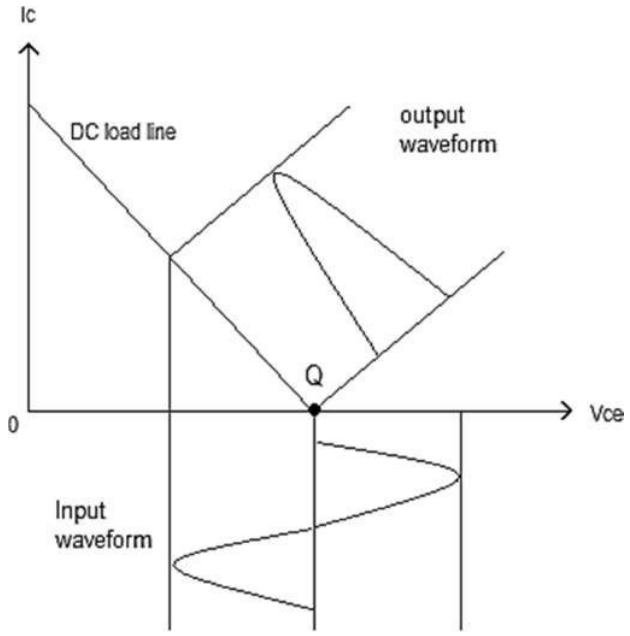
Class B power amplifier:

Class B amplifier is a type of power amplifier where the active device (transistor) conducts only for one half cycle of the input signal. That means the conduction angle is 180° for a Class B amplifier. Since the active device is switched off for half the input cycle, the active device dissipates less power and hence the efficiency is improved. Theoretical maximum efficiency of Class B power amplifier is 78.5%. The schematic of a single ended Class B amplifier and input , output waveforms are shown in the figure below.



Single ended Class B amplifier

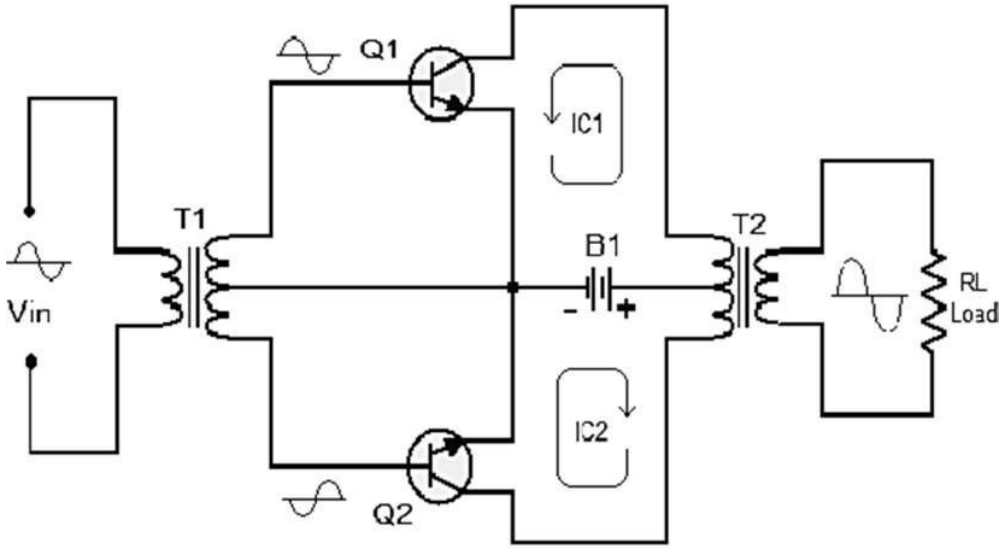
From the above circuit it is clear that the base of the transistor Q1 is not biased and the negative half cycle of the input waveform is missing in the output. Even though it improves the power efficiency, it creates a lot of distortion. Only half the information present in the input will be available in the output and that is a bad thing. Single ended Class B amplifiers are not used in present day practical audio amplifier application and they can be found only in some earlier gadgets. Another place where you can find them is the RF power amplifiers where the distortion is not a matter of major concern. Anyway, Class C amplifiers are more often used in RF power amplifier applications. Output characteristics of a single ended Class B power amplifier is shown in the figure below.



Class B power amplifier output characteristics

One way to realize a practical Class B amplifier is to use a pair of active devices (transistors) arranged in push-pull mode where one transistor conducts one half cycle and the other transistor conducts the other half cycle. The output from both transistors are then combined together to get a scaled replica of the input. But there is a snag – there must be some way to split the input wave form to feed the individual transistors and there must be some way to put together the output of the individual transistors. Transformer coupling is solution for this problem and such amplifiers are called transformer coupled Class B amplifiers.

Transformer coupled Class B amplifier:



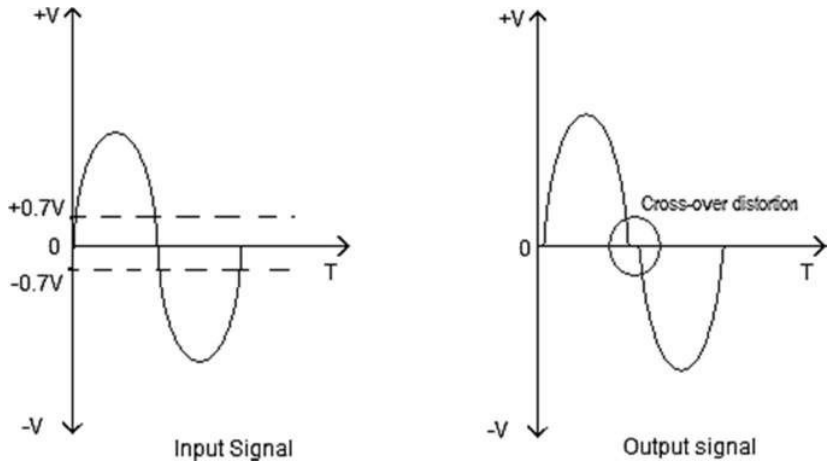
Transformer coupled Class B amplifier

The circuit diagram of a simple transformer coupled class B power amplifier is shown in the figure above. Transistor Q1 and Q2 are the active elements. The transformer T1 reproduces the input signal into two copies which are 180° out of phase. From the above figure you can see that the transistor Q1 amplifies the positive half of the input signal and transistor Q2 amplifies the negative half of the input signal. Current flow path of the two transistors are also depicted in the above figure. The amplified two halves are joined together by the transformer T2. If an ideal transformer is used the DC components of the collector current of each transistors will flow in opposite directions through the transformer primary and they will cancel each other. That means there is no core saturation and there will be no DC components in the output.

Since the transistors are not biased they remains OFF when there is no input signal and no current flows through the load. Each transistor starts conduction only when the amplitude of the input signal goes above the base-emitter voltage (Vbe) of the transistor which is about 0.7 V. This improves the efficiency but creates a problem called cross-over distortion.

Cross over distortion:

Since the active elements start conduction only after the input signal amplitude has risen above 0.7V, the regions of the input signal where the amplitude is less than 0.7V will be missing in the output signal and it is called cross over distortion. The schematic representation of cross-over distortion is shown in the figure below. In the figure, you can see that the regions of the input waveform which are under 0.7V are missing in the output waveform.



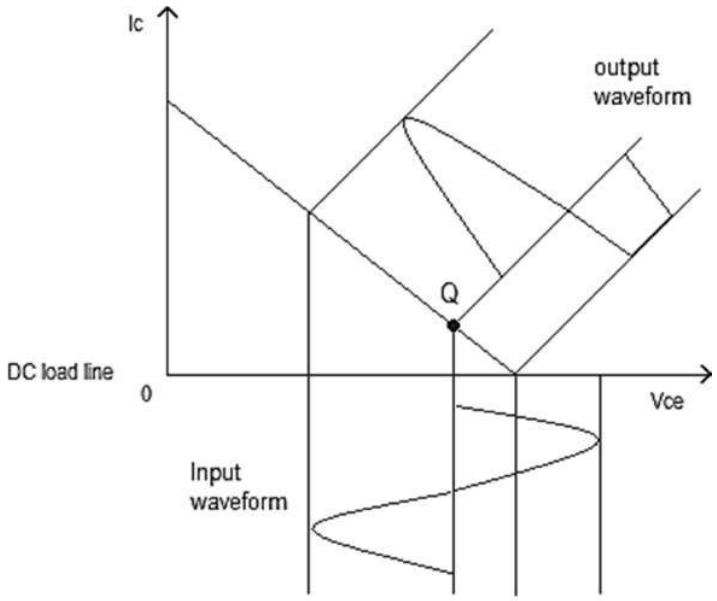
Advantages of Class B amplifier:

- High efficiency when compared to the Class A configurations.
- Push-pull mechanism avoids even harmonics.
- No DC components in the output (in ideal case).

Disadvantages of Class B amplifier:

- The major disadvantage is the cross-over distortion.
- Coupling transformers increases the cost and size.
- It is difficult to find ideal transformers.
- Transformer coupling causes hum in the output and also affects the low frequency response.
- Transformer coupling is not practical in case of huge loads. Class AB power amplifier:

In Class AB configuration, the active elements (transistors) are slightly biased so that the conduction angle is slightly more than 180° but much less than 360°. The transistors conduct for more than a half cycle but much less than the full cycle. That means there will be no instant where both transistors are OFF simultaneously and thus cross-over distortion is eliminated. Class AB configuration is actually a trade-off between Class A and Class B configurations where efficiency is slightly compromised for fidelity. Class AB power amplifiers are slightly inefficient than the Class B configurations but far better in terms of distortion when compared to Class A configurations. Since the active devices are slightly pre-biased there will be a small amount of collector current flowing and this is the reason behind the slightly reduced efficiency. Typical efficiency of a well designed class AB power amplifier is around 70%. The output characteristics of a single ended Class AB power amplifier is shown in the figure below.

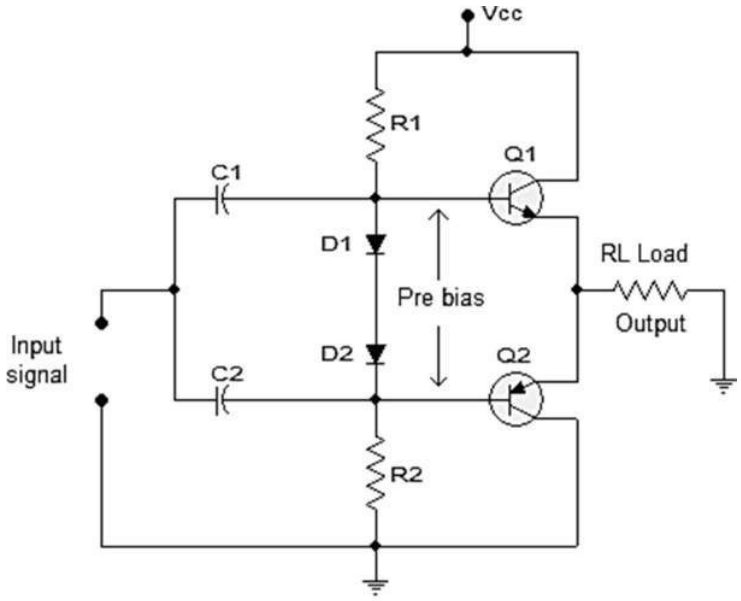


Class AB power amplifier output characteristics

From the above figure it is clear that the Q-point is not positioned at cut-off unlike the Class B characteristics and there will be a small amount of collector current flowing at zero input. As a result, some part of the negative going half cycle will be also reproduced at the output. The amount of negative going half cycle reproduced at the output depends on the amount of pre-bias given to the transistor.

Practical Class AB power amplifier:

Single ended Class AB configurations are not practical just because a major portion of one half cycle will be missing at the output. Just like the Class B configuration, push-pull mechanism is essential for realizing practical Class AB power amplifiers. Circuit diagram of a typical Class AB push-pull amplifier is shown in the figure below.

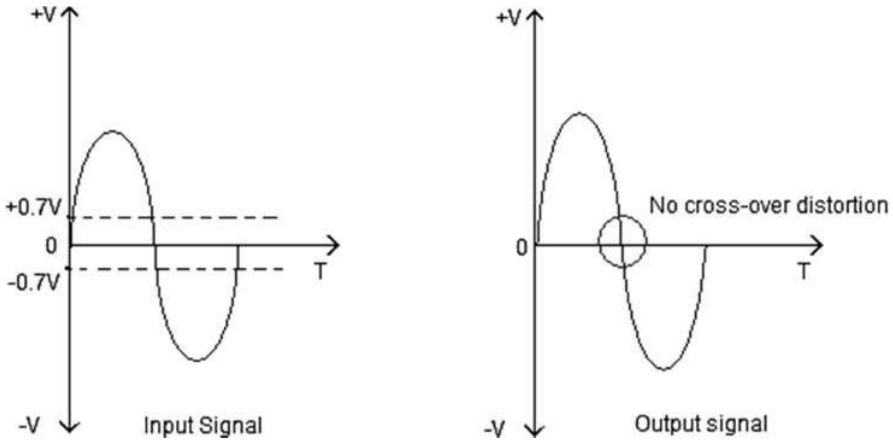


Class AB push-pull amplifier

The exact technical designation of the above circuit is " Complementary- symmetry Class AB power amplifier". The active elements used in this circuit (transistor Q1 and Q2) are complementary symmetric and it means the transistor are similar in all aspects except one is NPN and the other is PNP. The use of this complementary pair eliminates the bulky transformer for phase splitting the input signal for driving the individual transistors. The NPN transistor alone will conduct the positive half cycle and PNP transistor alone will conduct the negative half cycle.

Slight pre-biasing is given to the transistors using the network comprising of resistors R1, R2 and biasing diodes D1 and D2. As you know, an NPN transistor will start conducting when its base voltage is above the base emitter voltage (Vbe~0.7V) and a PNP transistor will start conducting when its base voltage is below the base emitter voltage (Vbe~ -0.7V). A forward biased diode will drop approximately 0.7V across it and the biasing diodes used here will keep the transistor slightly forward biased even if there is no input signal.

One important thing while choosing the biasing diodes (also called compensating diodes) is that their characteristics must match as close as possible to the transistors. Resistors R1 and R2 are actually used for forward biasing the diodes so that they drop 0.7V across it for biasing the individual transistors. C1 and C2 are input DC decoupling capacitors. Input and output waveforms of a typical class AB push pull amplifier is shown in the figure below.



Since both the transistors are slightly conducting at zero input, no information in the input signal is lost at the output during the zero-crossing of the input signal and thus cross-over distortion is completely eliminated at a cost of slightly reduced efficiency.

Advantages of Class AB power amplifier:

- No cross over distortion.
- No need for the bulky coupling transformers.
- No hum in the output.

Disadvantages of Class AB power amplifier:

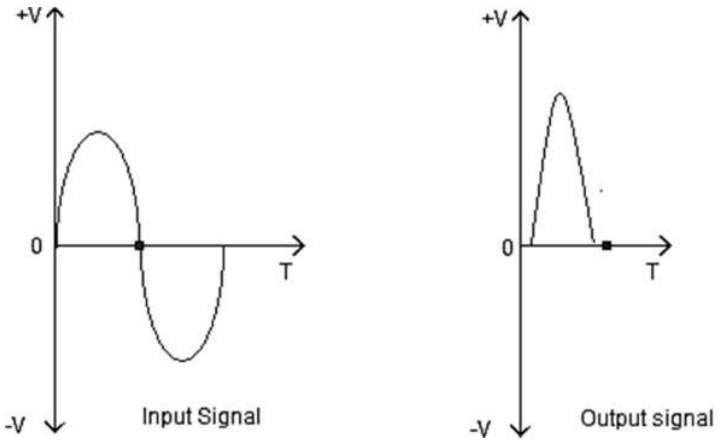
- Efficiency is slightly less when compared to Class B configuration.
- There will be some DC components in the output as the load is directly coupled.
- Capacitive coupling can eliminate DC components but it is not practical in case of heavy loads.

Class C power amplifier:

Class C power amplifier is a type of amplifier where the active element (transistor) conduct for less than one half cycle of the input signal. Less than one half cycle means the conduction angle is less than 180° and its typical value is 80° to 120°. The reduced conduction angle improves the efficiency to a great extend but causes a lot of distortion. Theoretical maximum efficiency of a Class C amplifier is around 90%.

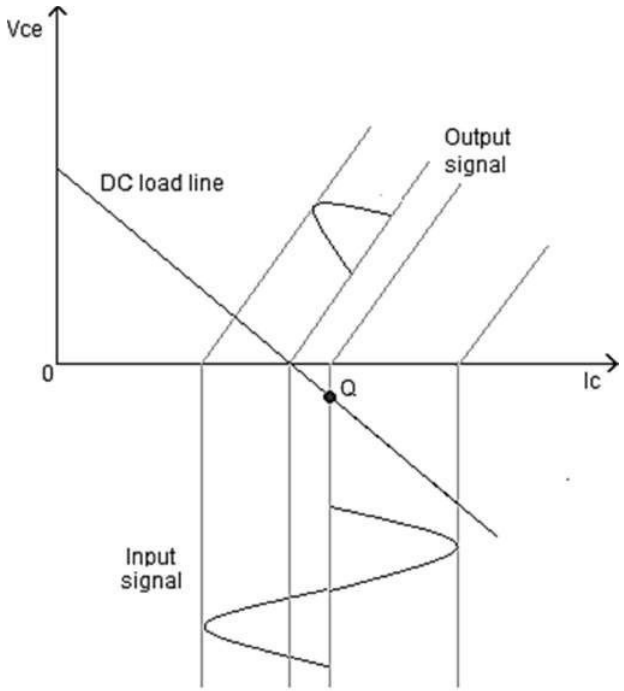
Due to the huge amounts of distortion, the Class C configurations are not used in audio applications. The most common application of the Class C amplifier is the RF (radio frequency) circuits like RF oscillator, RF

amplifier etc where there are additional tuned circuits for retrieving the original input signal from the pulsed output of the Class C amplifier and so the distortion caused by the amplifier has little effect on the final output. Input and output waveforms of a typical Class C power amplifier is shown in the figure below.



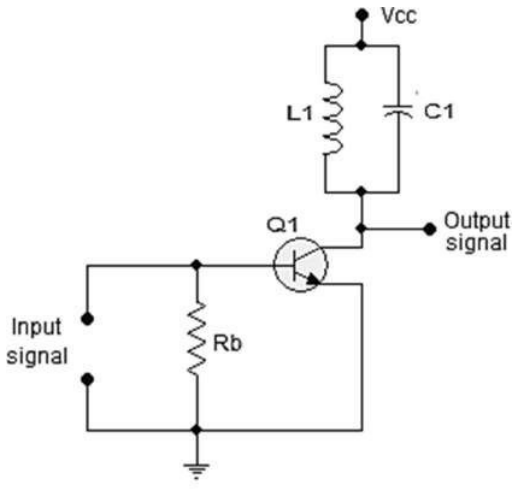
From the above figure it is clear that more than half of the input signal is missing in the output and the output is in the form of some sort of a pulse.

Output characteristics of Class C power amplifier:



Class C power amplifier output characteristics

In the above figure you can see that the operating point is placed some way below the cut-off point in the DC load-line and so only a fraction of the input waveform is available at the output. Class C power amplifier circuit diagram:



Class C power amplifier

Biasing resistor Rb pulls the base of Q1 further downwards and the Q-point will be set some way below the cut-off point in the DC load line. As a result the transistor will start conducting only after the input

signal amplitude has risen above the base emitter voltage (Vbe~0.7V) plus the downward bias voltage caused by Rb. That is the reason why the major portion of the input signal is absent in the output signal. Inductor L1 and capacitor C1 forms a tank circuit which aids in the extraction of the required signal from the pulsed output of the transistor. Actual job of the active element (transistor) here is to produce a series of current pulses according to the input and make it flow through the resonant circuit. Values of L1 and C1 are so selected that the resonant circuit oscillates in the frequency of the input signal. Since the resonant circuit oscillates in one frequency (generally the carrier frequency) all other frequencies are attenuated and the required frequency can be squeezed out using a suitably tuned load. Harmonics or noise present in the output signal can be eliminated using additional filters. A coupling transformer can be used for transferring the power to the load.

Advantages of Class C power amplifier:

- High efficiency.
- Excellent in RF applications.
- Lowest physical size for a given power output.

Disadvantages of Class C power amplifier:

- Lowest linearity.
- Not suitable in audio applications.
- Creates a lot of RF interference.
- It is difficult to obtain ideal inductors and coupling transformers.
- Reduced dynamic range.

Applications of Class C power amplifier:

- RF oscillators.
- RF amplifier.
- FM transmitters.
- Booster amplifiers.
- High frequency repeaters.
- Tuned amplifiers etc.

Module VIII: Multivibrators:

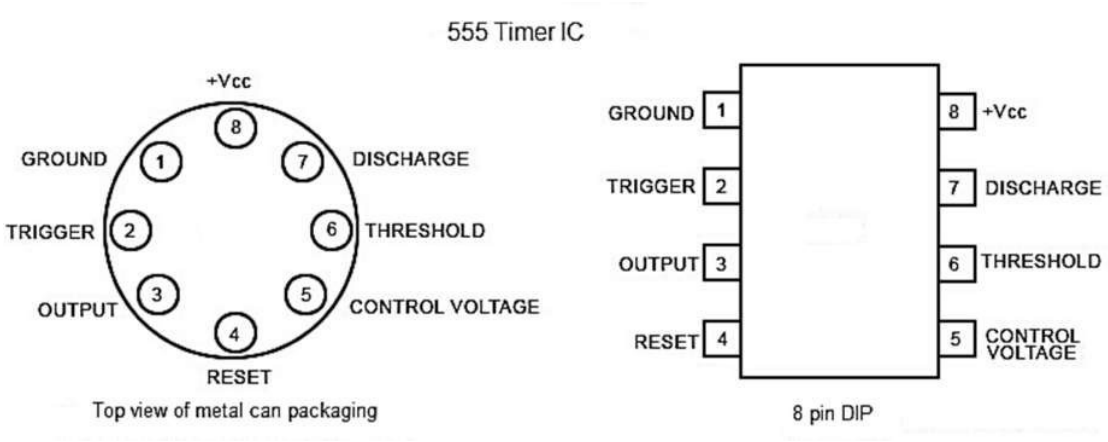
Introduction:

The 555 timer IC was introduced in the year 1970 by Signetic Corporation and gave the name SE/NE 555 timer. It is basically a monolithic timing circuit that produces accurate and highly stable time delays or oscillation. When compared to the applications of an op-amp in the same areas, the 555IC is also equally reliable and is cheap in cost. Apart from its applications as a monostable multivibrator and astable multivibrator, a 555 timer can also be used in dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control devices, voltage regulators etc. The timer IC is setup to work in either of the two modes – one-shot or monostabl or as a free-running or astablemultivibrator.The SE 555 can be used for temperature ranges between – 55°C to 125° . The NE 555 can be used for a temperature range between 0° to 70°C.

The important features of the 555 timer are :

- It operates from a wide range of power supplies ranging from + 5 Volts to + 18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilo hertz.
- The output of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005 %/°C.
- The duty cycle of the timer is adjustable.
- The maximum power dissipation per package is 600 mW and its trigger and reset inputs has logic compatibility.

IC Pin Configuration:



The 555 Timer IC is available as an 8-pin metal can, an 8-pin mini DIP (dual-in-package). The pin configuration is shown in the figures.

Pin 1: Grounded Terminal: All the voltages are measured with respect to the Ground terminal.

Pin 2: Trigger Terminal: The trigger pin is used to feed the trigger input hen the 555 IC is set up as a monostable multivibrator. This pin is an inverting input of a comparator and is responsible for the transition of flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. A negative pulse with a dc level greater than Vcc/3 is applied to this terminal. In the negative edge, as the trigger passes through Vcc/3, the output of the lower comparator becomes high and the complimentary of Q becomes zero. Thus the 555 IC output gets a high voltage, and thus a quasi stable state.
Pin 3: Output Terminal: Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the normally on load and that connected between output and ground pin is called the normally off load.

Pin 4: Reset Terminal: Whenever the timer IC is to be reset or disabled, a negative pulse is applied to pin 4, and thus is named as reset terminal. The output is reset irrespective of the input condition. When this pin is not to be used for reset purpose, it should be connected to + V_{CC} to avoid any possibility of false triggering.

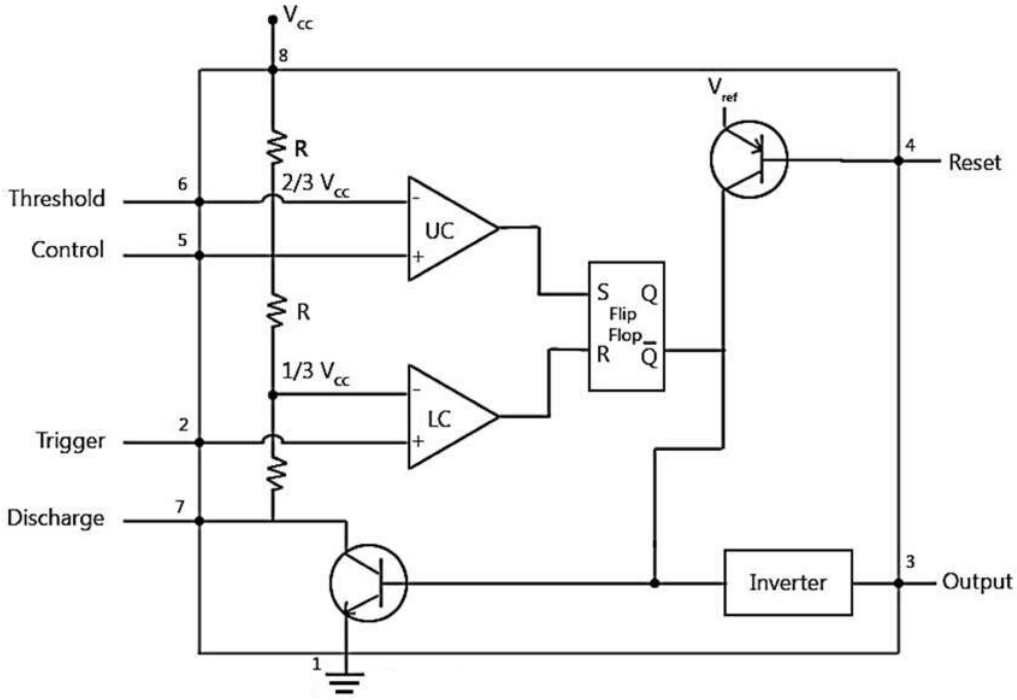
Pin 5: Control Voltage Terminal: The threshold and trigger levels are controlled using this pin. The pulse width of the output waveform is determined by connecting a POT or bringing in an external voltage to this pin. The external voltage applied to this pin can also be used to modulate the output waveform. Thus, the amount of voltage applied in this terminal will decide when the comparator is to be switched, and thus changes the pulse width of the output. When this pin is not used, it should be bypassed to ground through a 0.01 micro Farad to avoid any noise problem.

Pin 6: Threshold Terminal: This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. The amplitude of voltage applied to this terminal is responsible for the set state of flip-flop. When the voltage applied in this terminal is greater than 2/3Vcc, the upper comparator switches to +Vsat and the output gets reset.

Pin 7: Discharge Terminal: This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

Pin 8: Supply Terminal: A supply voltage of + 5 V to + 18 V is applied to this terminal with respect to ground (pin 1).

Block diagram of 555 IC Timer



The block diagram of a 555 timer is shown in the above figure. A 555 timer has two comparators, which are basically 2 op-amps), an R-S flip-flop, two transistors and a resistive network.

- Resistive network consists of three equal resistors and acts as a voltage divider.
- Comparator 1 compares threshold voltage with a reference voltage + $2/3V_{CC}$ volts.
- Comparator 2 compares the trigger voltage with a reference voltage + 1/3 V_{CC} volts.

Output of both the comparators is supplied to the flip-flop. Flip-flop assumes its state according to the output of the two comparators. One of the two transistors is a discharge transistor of which collector is connected to pin 7. This transistor saturates or cuts-off according to the output state of the flip-flop. The saturated transistor provides a discharge path to a capacitor connected externally. Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the whole timer irrespective of any input.

Working Principle:

Refer Block Diagram of 555 timer IC given above:

The internal resistors act as a voltage divider network, providing (2/3)Vcc at the non-inverting terminal of the upper comparator and (1/3)Vcc at the inverting terminal of the lower comparator. In most applications, the control input is not used, so that the control voltage equals +(2/3) V_{CC}. Upper comparator has a threshold input (pin 6) and a control input (pin 5). Output of the upper comparator is applied to set (S) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the upper comparator will set the flip-flop and its output is high. A high output from the flip-flop when given to the base of the discharge transistor saturates it and thus discharges the transistor that is connected externally to the discharge pin 7. The complementary signal out of the flip-flop goes to pin 3, the output. The output available at pin 3 is low. These conditions will prevail until lower comparator triggers the flip-flop. Even if the voltage at the threshold input falls below (2/3)V_{CC}, that is upper comparator cannot cause the flip- flop to change again. It means that the upper comparator can only force the flip-flop's output high.

To change the output of flip-flop to low, the voltage at the trigger input must fall below + (1/3) Vcc. When this occurs, lower comparator triggers the flip-flop, forcing its output low. The lowoutput from the flip-flop turns the discharge transistor offand forces the power amplifier to output a high. These conditions will continue independent of the voltage on the trigger input. Lower comparator can only cause the flip-flop to output low.

From the above discussion it is concluded that for the having low output from the timer 555, the voltage on the threshold input must exceed the control voltage or + (2/3)V_{CC}. This also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below +(1/3)V_{CC}. This turns the discharge transistor off.

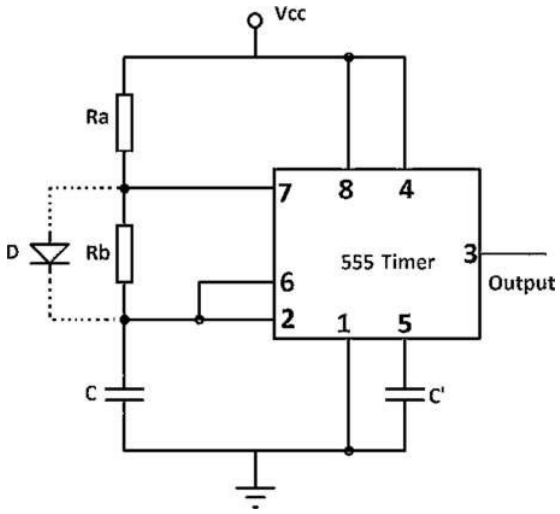
A voltage may be applied to the control input to change the levels at which the switching occurs. When not in use, a 0.01 nano Farad capacitor should be connected between pin 5 and ground to prevent noise coupled onto this pin from causing false triggering.

Connecting the reset (pin 4) to a logic low will place a high on the output of flip-flop. The discharge transistor will go on and the power amplifier will output a low. This condition will continue until reset is taken high. This allows synchronization or resetting of the circuit's operation. When not in use, reset should be tied to +V_{CC}.

Astable Multivibrator:

An AstableMultivibrator is an oscillator circuit that continuously produces rectangular wave without the aid of external triggering. So astable multivibrator is also known as Free Running multivibrator. Astable multivibrator using 555 Timer is very simple, easy to design, very stable and low cost. It can be used for timing from microseconds to hours. Due to these reasons 555 has a large number of applications and it is a popular IC among electronics hobbyists.

Astable multivibrator using I.C 555 – Circuit:



above figure shows the circuit diagram of a 555 Timer wired in astable Mode. 8th pin and 1st pin of the IC are used to give power, Vcc and GND respectively. The 4th pin is RESET pin which is active low and is connected to Vcc to avoid accidental resets. 5th pin is the Control Voltage pin which is not used. So to avoid high frequency noises it is connected to a capacitor C' whose other end is connected to ground. Usually C' = 0.01µF. The Trigger (pin 2) and Threshold (pin 6) inputs are connected to the capacitor which determines the output of the timer. Discharge pin (pin 7) is connected to the resistor Rb such that the capacitor can discharge through Rb. Diode D connected in parallel to Rb is only used when an output of duty cycle less than or equal to 50% is required.

Design Equations: Capacitor Charges through Ra and Rb.

Thigh = 0.693(Ra + Rb)C

Capacitor Discharges through Rb

- Tlow = 0.693RbC
- Output Frequency = 1/(Tlow + Thigh) = 1.44/((Ra + 2Rb) * C)
- Duty Cycle = Thigh/(Thigh + Tlow)

Where Thigh and Tlow are the time period of HIGH and LOW of the output of 555.

From this we can find that Duty Cycle less than or equal to 50% cannot be obtained. There are two ways to obtain this.

1. Inverting the output
2. Using a Diode Parallel to resistor Rb

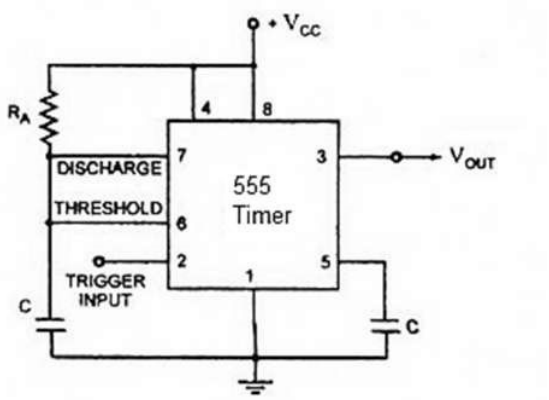
1. Inverting the Output: In this method, just compliment the output. Thus the Duty Cycle = T low/ (T low + Thigh). Where T low and Thigh are the time period of LOW and HIGH of output of 555. In this method the duty cycle of the output of 555 will be greater than 50% and that of inverter will be less than 50%. Duty Cycle of 555 = 1 – Duty Cycle of Inverter

2. Using a Diode Parallel to resistor Rb: In this method we will connect a diode parallel to resistor Rb as shown dotted in the first circuit diagram above. Thus the charging current of capacitor will bypass the resistorRb. Thus Thigh=0.693RaC

Thus a Duty Cycle less than or equal to 50% can easily obtained.

Monostable Multivibrator:

A monostable multivibrator (MMV) often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable). For auto- triggering of output from quasi-stable state to stable state energy is stored by an externally connected capacitor C to a reference level. The time taken in storage determines the pulse width. The transition of output from stable state to quasi-stable state is accomplished by external triggering. The schematic of a 555 timer in monostable mode of operation is shown in figure.

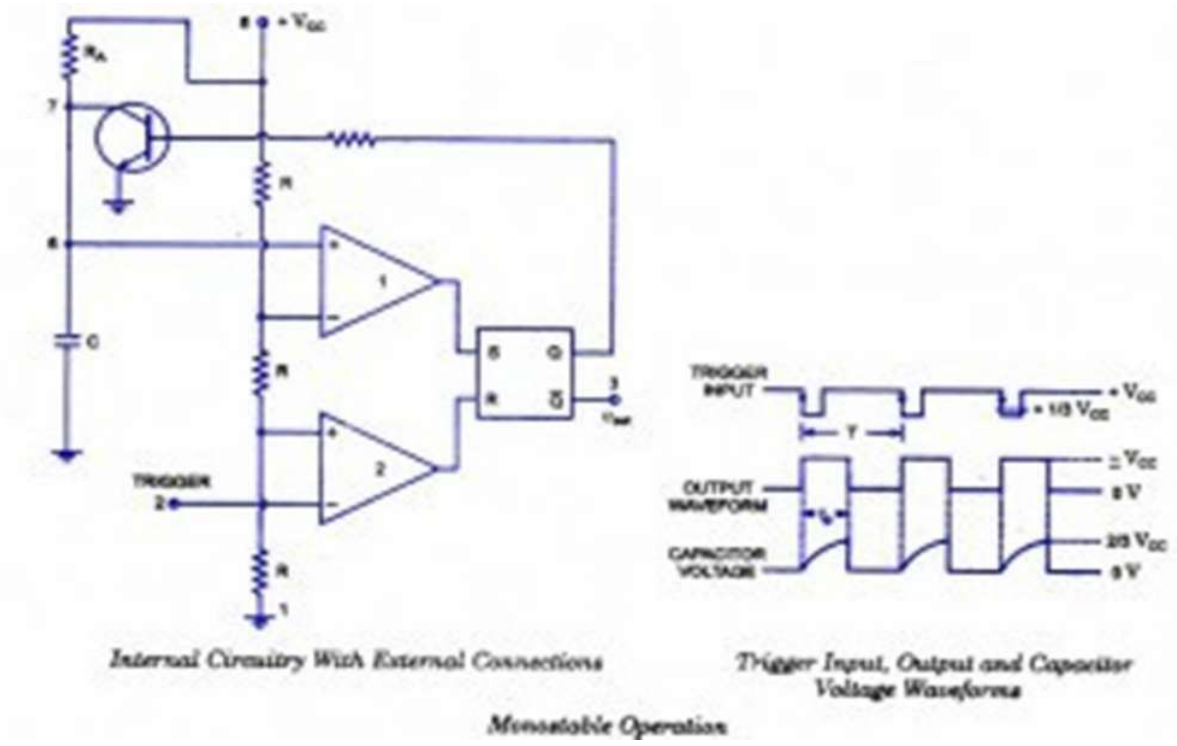


555 timer as monostable multivirator

MonostableMultivibrator Circuit details:

Pin 1 is grounded. Trigger input is applied to pin 2. In quiescent condition of output this input is kept at+ V_{CC}. To obtain transition of output from stable state to quasi-stable state, a negative-going pulse of narrow width (a width smaller than expected pulse width of output waveform) and amplitude of greater than + 2/3 V_{CC} is applied to pin 2. Output is taken from pin 3. Pin 4 is usually connected to + V_{CC} to avoid accidental reset. Pin 5 is grounded through a 0.01 u F capacitor to avoid noise problem. Pin 6 (threshold) is shorted to pin 7. A resistor R_A is connected between pins 6 and 8. At pins 7 a discharge capacitor is connected while pin 8 is connected to supply V_{CC}.

555 IC MonostableMultivibrator Operation:



Internal Circuitry With External Connections

Trigger Input, Output and Capacitor Voltage Waveforms

Monostable Operation

For explaining the operation of timer 555 as a monostable multivibrator, necessary internal circuitry with external connections are shown in figure.

The operation of the circuit is explained below:

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor- C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 V_{CC}, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward $+V_{CC}$ through resistance R_A with a time constant equal to R_AC. When the increasing capacitor voltage becomes slightly greater than +2/3 V_{CC}, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure. Thus the output returns back to stable state from quasi-stable state. The output of the monostable multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats. Trigger input, output voltage and capacitor voltage waveforms are shown in figure.

Monostable Multivibrator Design Using 555 timer IC:

The capacitor C has to charge through resistance R_A. The larger the time constant R_AC, the longer it takes for the capacitor voltage to reach $+2/3V_{CC}$.

In other words, the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

$t_p = 1.0986\ R_AC$ where R_A is in ohms and C is in farads. The above relation is derived as below. Voltage across the capacitor at any instant during charging period is given as

$v_c = V_{CC}\ (1 - e^{-t/R_AC})$

Substituting $v_c = 2/3\ V_{CC}$ in above equation we get the time taken by the capacitor to charge from 0 to $+2/3V_{CC}$.

So $+2/3V_{CC}. = V_{CC}. (1 – e^{–t/RAC})$ or $t – R_AC \log_e 3 = 1.0986\ R_AC$

So pulse width, $t_P = 1.0986\ R_AC$ s $1.1\ R_AC$

The pulse width of the circuit may range from micro-seconds to many seconds. This circuit is widely used in industry for many different timing applications.

Module IX: Special function circuits:

VCO:

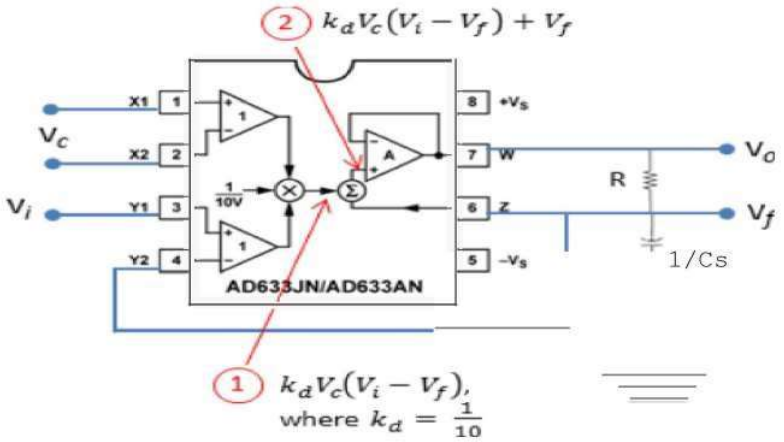
Voltage-controlled oscillators are specialized oscillators in which the oscillation frequency varies with a control voltage. VCOs are used in many communication applications such as frequency modulason, in the phase locked loop (PL L) for signal tracking and PM demodulation. There are many ways to design an electronic circuit for a VCO. One method uses a special diode called Varactor. This diode has capacitance that varies with the applied voltage. As the capacitance varies the applied voltage so does the hme constant of the oscillator resulting in an output signal with varying frequency. VC O can also be designed by making the hmm DDIlStdSlt Df the capacitor dependCnt upDn a cDntrDl voltage. In this assignment you'll build a VCO using the analog nniltiplier used in AM modulator (AD633) and a high frequency op-amp chip (AD9 631). You'll also study the phase locked loop and a commercially available VC O (CD4046).

Pigure 1 shows a functional diagram of an RC circuit using the analog multiplier chip ADh33. We are interested in finding transfer function of this circuit with respect to the input V, and output Vt. By examining Pig. 1 we can write the expressions for Vtand Vp, which are as follows:

$$F=k \quad F,(F,-Fy)+Fy \tag{1}$$

$$V_f = \frac{\frac{1}{Cs}}{R+\frac{1}{Cs}} V_o = \frac{1}{RCs+1} V_o \tag{2}$$

$$V_o = (RCs+1)V_f \tag{3}$$



Equating Eqs, (1) and (3) welds

$$(Rcs+i)vy \text{—} k,z,(v,-vy)+vy \tag{4}$$

Of

$$RCsV_f + V_f = k_d V_c V_i - k_d V_c V_f + V_f \tag{5}$$

Of

$$RCsV_f + k_d V_c V_f = k_d V_c V_i \tag{6}$$

Of

$$\frac{V_f}{V_i} = \frac{k_d V_c}{RCs + k_d V_c} \tag{7}$$

OI

$$\frac{V_f}{V_i} - \frac{\frac{k_d V_c}{RC}}{s + \frac{k_d V_c}{RC}} \tag{8}$$

Equation (8) represents the transfer function (with respect to the output ¥ r) of a low-pass filter (LPF) that has a pole at

—

That means the location of the pole and, therefore, the break frequency of the LPF depends on the control voltage V_c. If we incorporate the circuit of Fig. 1 into a relaxation oscillator we can build an oscillator that has output frequency changing with the control voltage V_c. This kind of oscillator is called a voltage-controlled oscillator or VCO. VCOs are commonly used in frequency modulation (FM) and demodulation as well as phase-locked loop (PLL) circuits.

Phase-Locked Loop (PLL)

Phase-locked loop (PLL) é a feedback system consisting of a voltage-controlled oscilhtor, a phase comparator, and a loop filter and shown in Figure S. The phase comparator compares the pfiase of the reference signal with the pfiase of the output of voltage control oscillator and genaates an error signa[wfiicfi is pmportional to the pfiase difference between the refaence input and the output of the voltage controlled oscillator. The error signal is used as a control voltage to the voltage controlled oscillator. Tfie voltage controlled oscillator changes the frequency of its output based on the error signal. Tfie cfiange in the fiequency of the output of the voltage controlled oscillator is in the déection that reduces the difference in the frequency of the reference input and the ouQut of the voltage controlled oscillator. 7he negative feedback causes the error signal to eventually appmach zen, at whicfi point the frequency of the output of the voltage controlled oscillator becomes the same as the hequency of the reference input and the frequency is said to be *locked.*

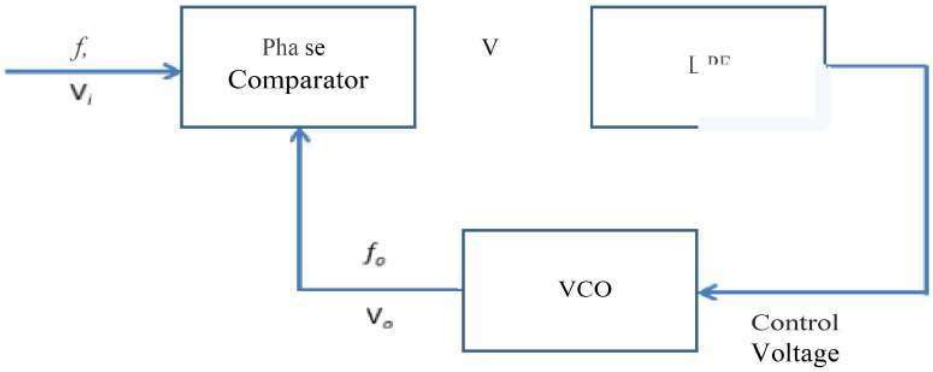


Figure 5: Functional diagram of the phase-locked loop.