GURU NANAK INSTITUTE OF TECHNOLOGY

An Autonomous Institute under MAKAUT

2020-2021

Digital Electronics and Computer Organization (Backlog)

CS302

TIME ALLOTTED: 3 Hrs **FULL MARKS: 70**

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable

GROUP – A

(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

		Marks	CO No.
1(i)	Convert the following SOP expression to an equivalent POS expression. $A\,B\,C + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + A\,B\,\overline{C} + \overline{A}\,\overline{B}\,C$ a $(\overline{A} + \overline{B} + \overline{C})(A + B + \overline{C})(\overline{A} + B + C)$ b. $(A + B + C)(A + \overline{B} + C)(A + \overline{B} + \overline{C})$ c. $(\overline{A} + \overline{B} + \overline{C})(A + \overline{B} + C)(A + \overline{B} + C)$ d. $(A + B + C)(\overline{A} + B + \overline{C})(A + \overline{B} + C)$	1	CO1
1(ii)	Microinstructions are kept in a. Main memory b. cache memory c. control memory d. none of these	1	CO5
1(iii)	(A+B′+A′B)C is same as a. 1 b. 0 c. C d. C′	1	CO1
1(iv)	Which of the following addressing mode is used for the instruction "Push B" ? a. Register b. Register indirect c. Direct d. Immediate	1	CO2
1(v)	Let $\oplus$ and $\odot$ denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT correct? a. $(P \oplus Q)' = P \odot Q$ b. $P' \oplus Q = P \odot Q$ c. $P' \oplus Q' = P \oplus Q$ d. $(P \oplus P') \oplus Q = (P \odot P') \odot Q'$	1	CO1

1(vi)	The minimum number of flip flops required to design a MOD-10 counter is a. 3 b. 5 c. 4 d. 10	1	CO4
1(vii)	The minimum no. of NAND gates required to design one half adder circuit is a. 5 b. 8 c. 10 d. 9	1	CO3
1(viii)	The logic circuit in ALU is a. entirely combinational b. combinational and sequential c. entirely sequential d. none of these	1	CO2
1(ix)	In DMA, cycle stealing means a. Controller gets opportunity to transfer only one word in a time slot b. CPU releases the bus and DMA controller can use endlessly c. 100 bytes are allowed to be transferred d. None of these	1	CO5
1(x)	To construct an n-line common bus using MUX for k registers of n bits each, the number of MUXs and size of each MUX are a. k and n x1 b. n and 2^k c. n and kx1 d. k and 2^n	1	CO3
1(xi)	The race around condition occurs in a. JKFF b. SRFF c. Master Slave FF d. DFF	1	CO4
1(xii)	What is the control unit's function in the CPU? a. To transfer data to primary storage b. to store program instruction c. to perform logic operations d. to decode program instruction	1	CO2

GROUP – B
(Short Answer Type Questions)

(Answer any *three* of the following) **3 x 5 = 15**

		Marks	**CO No.**
2. a)	Distinguish between latch and flipflop.	2	CO4
2. b)	Explain Triggering of Flip-Flops with example.	3	CO4

3.a)	Represent -9.5 in 32-bit IEEE floating point representation.	3	CO2
3.b)	What are guard bits?	2	CO2
4.	What are the different types of DMA controllers?	5	CO5
5. a)	Distinguish between ripple counter and synchronous counter.	3	CO4
5. b)	Compare parallel adder with serial adder.	2	CO3
6.	Distinguish between Hardwired control unit and micro-programmed control unit.	5	CO5

GROUP – C
(Long Answer Type Questions)

(Answer any *three* of the following) **3 x 15 = 45**

		Marks	**CO No.**
7. a)	What is Von Neumann bottleneck?	2	CO2
7. b)	Explain the logic of a 4-bit carry look ahead adder with suitable diagram.	6	CO3
7. c)	Design the circuit of 3:8 Decoder and verify its truth table.	6	CO3
7.d)	Design a comparator circuit with suitable truth table and diagram.	3	CO3
8. a)	Describe JK Flip-Flop with truth table and characteristics table.	5	CO4
8. b)	Construct a D flip-flop using S-R flip-flop. Explain its characteristic table and excitation table.	4	CO4
8. c)	Minimize the following expression in POS form using K-map and realize the simplified expression using NOR gates only. $Y(A, B, C, D) = \Pi(0,1,4,5,6,8,9,12,13,14)$	6	CO1
9. a)	Design a 4-bit asynchronous up-down counter.	6	CO4
9. b)	Design a MOD-N synchronous binary UP-counter using JK flip-flop & other necessary logic gates.	6	CO4
9. c)	Design a 4-bit bidirectional shift register.	3	CO4
10. a)	Apply non-restoring division algorithm to divide 9 by 3.	6	CO2
10. b)	Draw and explain instruction state cycle.	4	CO2
10. c)	An instruction is stored at location 300 with its address field at location 301.The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.	5	CO2
11.	Write short notes on any three of the following:	3x5	
11. a)	IOP	5	CO5
11.b)	Ring counter	5	CO4
11.c)	SRAM and DRAM.	5	CO5
11.d)	DE-MUX	5	CO3
11.e)	Tri state buffer.	5	CO3