GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2020-2021
VLSI AND MICROELECTRONICS
EC702

TIME ALLOTTED: 3 HOURS **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

Answer any *ten* from the following, choosing the correct alternative of each question: 10×1=10

			Marks	CO No
1.	(i)	The advantage of IC over discrete component-based circuits is (a) low power (b) small size (c) low cost (d) all of these	1	CO1
	(ii)	FPGA-based design is more suitable for (a) prototype development (b) large scale product development (c) low power application (d) high speed application	1	CO1
	(iii)	For a 0.5 μm process technology _____. (a) $\lambda = 0.5$ μm (b) $\lambda = 0.25$ μm (c) $\lambda = 1$ μm (d) $\lambda = 0.125$ μm	1	CO5
	(iv)	The equivalent resistance of a switched capacitor is _____. (a) proportional to capacitance (b) proportional to the square of the capacitance (c) inversely proportional to the capacitance (d) inversely proportional to the square of the capacitance	1	CO1
	(v)	The threshold voltage (Vth) of a CMOS inverter is defined (a) When $V_{in} \neq V_{out}$ (b) When $V_{in} = V_{out}$ (c) When $V_{in} = 0.5V_{out}$ (d) When $V_{in} = 2V_{out}$	1	CO2
	(vi)	The VTC curve of a CMOS inverter determines (a) Noise margin of the gate (b) Threshold voltage (c) V_{OL}, V_{OH}, V_{IL}, V_{IH} (d) All of these	1	CO2

(vii)	An ideal current source is a two-terminal element whose current (a) is constant for any voltage across the source (b) is monotonically decreased with the increase of voltage across the source (c) is monotonically increased with the increase of voltage across the source (d) none of these	1	CO3
(viii)	The smallest feature size (lambda or λ) used to measure an IC is _____ . (a) half the length of the smallest transistor (b) two-thirds the length of the smallest transistor (c) one-fourth the length of the smallest transistor (d) none of the above	1	CO5
(ix)	The critical path in a design refers to (a) the path having maximum delay (b) a path with minimum delay (c) the path having optimum delay (d) a path with no delay	1	CO6
(x)	AND terms are realized by _____ connections of nMOS in PDN. (a) cascade (b) parallel (c) series (d) anti-parallel	1	CO2
(xi)	_____ can pass a logic 0 perfectly, but cannot pass a logic 1 perfectly. (a) nMOS transistor (b) pMOS transistor (c) CMOS transistor (d) none of these	1	CO2
(xii)	Pull-down network (PDN) connects output node to _____. (a) V_{DD} (b) ground (c) input (d) all of these	1	CO2

GROUP – B
(Short Answer Type Questions)
Answer any *there* from the following: 3×5=15

			Marks	CO No
2.	(a)	What do you mean by MOSFET scaling?	2	CO1
	(b)	What are the different types of scaling techniques?	3	CO1
3.	(a)	Draw the Y-chart and explain the VLSI design process.	4	CO1
	(b)	What do you mean by set-up time and hold time of a flip-flop	1	CO6
4.	(a)	Define noise margins.	2	CO2

	(b)	Draw a stick diagram of CMOS NAND gate.	3	CO5
5.	(a)	Design the 4:1 MUX using TG.	4	CO2
	(b)	Define CMRR of CMOS OPAMP	1	CO4
6.	(a)	Design an XOR Gate using DCVSL technique	3	CO2
	(b)	What are the basic advantages of a switched capacitor?	2	CO3

GROUP – C
(Long Answer Type Questions)
Answer any *three* from the following: 3×15=45

			Marks	CO No
7.	(a)	Classify the different types of ASIC design	3	CO1
	(b)	What are the short channel effects? Discuss them in detail.	6	CO1
	(c)	Derive an expression for saturated drain current considering channel length modulation	6	CO1
8.	(a)	What is dynamic power dissipation in CMOS circuits? Does it depend on the power supply voltage? If so, explain how.	5	CO6
	(b)	Show that for a symmetric inverter the two-noise margin are same and are equal to VIL. Also show that for an ideal inverter $(W/L)_P=2.5(W/L)_N$.	5	CO2
	(c)	Draw the circuit of a CMOS full-adder circuit and explain its operation.	5	CO2
9.	(a)	What are current sources and current sinks?	4	CO3
	(b)	Why cascading is done in Current mirror? Explain with circuit diagram.	6	CO3
	(c)	Draw the CMOS differential amplifier circuit and explain how it works as a differential amplifier	5	CO4
10.	(a)	What do you mean by set-up time and hold time of a flip-flop? How can these problems occur in a design?	6	CO6
	(b)	What do you mean by 'Lambda Rule' & 'Micron Rule'? Draw the Layout & Schematic diagram of a Static CMOS NOR gate with identifying the corresponding components in the two drawing.	5	CO5
	(c)	Derive the expressions for rise and fall time of an inverter circuit.	4	CO6
11.		Write short notes on any three:		
	(a)	NORA logic	5	CO2
	(b)	Switched capacitor circuit	5	CO3
	(c)	FPGA architecture	5	CO1
	(d)	6T SRAM Cell	5	CO2
	(e)	Photo-lithography	5	CO5