GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2021
ADVANCED COMPUTER ARCHITECTURE
CS802D

TIME ALLOTTED: 3 Hours **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

			Marks	CO No.
1.	i)	A multiprocessor system with common shared memory is called: a) Loosely coupled system b) Tightly coupled system c) Both a and b d) None of the above	1	CO4
	ii)	Loosely coupled system are more efficient when the interaction between task is: a) Maximum b) Minimum c) Cannot say d) None of the above	1	CO4
	iii)	A bus that connects components in a multiprocessor system, is called: a) Control bus b) Data bus c) Address bus d) System bus	1	CO4
	iv)	MIPS stands for: a) Memory Instruction Per Second b) Major Instruction Per Second c) Main Information Per Second d) Million Instruction Per Second	1	CO1
	v)	The largest delay in accessing data on a disk is due to a) Seek time b) Rotation time c) data transfer time d) none of these	1	CO1

vi)	SPECint is a computer benchmark specification for a) Floating point performance testing component of the SPEC CPU testing suit. b) test of the CPU performance c) Integer performance testing component of the SPEC test suite. d)physical simulations	1	CO1
vii)	Static pipelines are preferred when a) several functional configurations exist simultaneously b) instructions of same type are to be executed continuously c) Both are true b) none is true	1	CO1
viii)	……. is the rate at which operations get executed. a) Latency b) Throughput c)Latch Latency d)None of the above		CO1
ix)	.....is a term used to denote a large class of techniques that are used to provide simultaneous data processing tasks a) Shared memory b) Parallel Processing c) Memory hierarchy d) None of the above		CO2
x)	Computers are interconnected with each other by means of communication lines to form a: a) Computer Network b) Multiprocessor c) Data Dependency d) None of the above	1	CO3
xi)	.....represents an organization that includes many processing units under the supervision of a common control unit. a) SISD b) SIMD c) MIMD d) None of the above	1	CO2
xii)	There are situations that prevent the next instruction in the instruction stream from being executing during its designated clock cycle is called a) Prefetching b) Hazard c) Functional dependency d) Interleaving	1	CO1

GROUP – B
(Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

			Marks	CO No.
2.	a)	What are the pipeline hazards?	2	CO1
	b)	How do they affect the speed up?	3	CO1
3.		What is speedup? Prove that a k stage pipeline can be at most k times faster than that of a non-pipelined system.	5	CO1
4.		Describe Cache Coherency in Shared Memory Machines.	5	CO4
5.	a)	What is multistage interconnection network?	2	CO3
	b)	Draw a 8X8 omega network.	3	CO3
6.		Explain Super-Scalar execution with the help of an example.	5	CO2

GROUP – C
(Long Answer Type Questions)

Answer any ***three*** from the following: **3×15=45**

			Marks	CO No.
7.	a)	Explain Throughput and speedup ratio of pipelined architecture.	2	CO1
	b)	State Amdahl's Law for maximum theoretical speedup.	2	CO1
	c)	Consider the following reservation table :	11	CO1

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
S1	X					X		X
S2		X		X				
S3			X		X		X	

i. Write down the forbidden latencies and initial collision vector.
ii. Draw the state diagram for scheduling the pipeline.
iii. Find out the simple cycle, greedy cycle and MAL.
iv. If the pipeline clock rate is 25 MHz, what is the throughput, efficiency and speed up of the pipeline?

8.	a)	Discuss on the following topics in detail: i. RISC Vs. CISC computer architecture ii. Pipelining vs. Parallelism	10	CO1
	b)	A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. Assuming constant clocking rate, i. What is the total time taken to process 1000 data items on this pipeline? ii. Compute the speedup, efficiency and throughput measure for this pipeline architecture.	5	CO1

9.	a)	What is embedded system and RTOS?	2	CO5
	b)	What are the important requirements that an OS meets to be considered as RTOS?	5	CO5
	c)	Give example of hard, soft and non-real time computing tasks. In what ways are they different?	5	CO5
	d)	Why preemptive multi-tasking is an important requirement for an RTOS?	3	CO5
10.	a)	Explain completely-connected and star networks?	5	CO3
	b)	What are the criteria that are used to evaluate the cost and performance of static interconnection networks?	5	CO3
	c)	What is shuffle-exchange function? What is its importance in interconnection network?	5	CO3
11.		**Write short notes: (Any three):**	3 X 5=15	
	a)	Flynn's classification	5	CO2
	b)	Embedded System Design Issues	5	CO5
	c)	Instruction set architecture (ISA)	5	CO1
	d)	Amdahl's law	5	CO4
	e)	Data flow & control flow computers	5	CO2
	f)	Data hazard	5	CO1