GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2021
COMPUTER ARCHITECTURE
CS401

TIME ALLOTTED: 3 HOURS **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

		Marks	CO No.
1(i)	A multiprocessor system with common shared memory is called: (a) Loosely coupled system (b) Tightly coupled system (c) Both a and b (d) None of the above	1	CO3
(ii)	When the addressed data/instruction is found in cache it is called: (a) Cache hit (b) Cache miss (c) Cache found (d) Cache trace	1	CO3
(iii)	How many smaller RAM chips of size 256X2 are required to construct a large RAM of size 1K X 8? (a) 4 (b) 16 (c) 64 (d) 32	1	CO2
(iv)	Associative memory is a (a) Pointer addressable memory (b) Content addressable memory (c) Very cheap memory (d) Slow memory	1	CO2
(v)	The largest delay in accessing data on a disk is due to (a) Seek time (b) Rotation time (c) data transfer time (d) none of these	1	CO2
(vi)	Floating point representation is used to store (a) Boolean values (b) Whole numbers (c) Real numbers (d) Integers	1	CO1

(vii)	Static pipelines are preferred when (a) several functional configurations exist simultaneously (b) instructions of same type are to be executed continuously (c) Both are true (d) none is true	1	CO1
(viii)	……. is the rate at which operations get executed. (a) Latency (b) Throughput (c) Latch Latency (d) None of the above	1	CO1
(ix)	Increasing the RAM of a computer typically improves performance because (a) Virtual memory increases (b) Larger RAM are faster (c) Fewer page faults occur (d) Fewer segmentation fault occur	1	CO2
(x)	The total size of address space in a virtual memory system is limited by (a) The length of MAR (b) The available secondary storage (c) The available main memory (d) All of the above	1	CO2
(xi)	.....represents an organization that includes many processing units under the supervision of a common control unit. (a) SISD (b) SIMD (c) MIMD (d) None of the above	1	CO2
(xii)	There are situations that prevent the next instruction in the instruction stream from being executing during its designated clock cycle is called (a) Prefetching (b) Hazard (c) Functional dependency (d) Interleaving	1	CO2

GROUP – B
(Short Answer Type Questions)

(Answer any *three* of the following) **3 x 5 = 15**

		Marks	**CO No.**
2.a)	Explain the different factors that affect performance of a pipelined system	3	CO2
b)	Differentiate between WAR and RAW hazards	2	CO2
3.a)	What do you mean by Throughput?	1	CO1
b)	What is prefetch buffer?	2	CO1

c)	Suppose that we are considering an enhancement that runs 10 times as faster than the original machine but is usable only 40% of the time. What is the overall speedup gained by incorporating the enhancement?	2	CO1
4.	We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?	5	CO1
5.a)	Explain the difference between superscalar and superpipelined architecture	2	CO3
b)	Briefly describe the VLIW processor architecture	3	CO3
6.	Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order- 3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24 Which of the memory blocks will not be in the cache at the end of the sequence?Also, calculate the hit ratio and miss ratio.	5	CO1

GROUP – C
(Long Answer Type Questions)

(Answer any *three* of the following) **3 x 15 = 45**

		Marks	**CO No.**
7.a)	Explain Throughput and speedup ratio of pipelined architecture.	2	CO1
b)	State Amdahl's Law for maximum theoretical speedup.	2	CO1
c)	Consider the following reservation table :	11	CO1

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
S1	X					X		X
S2		X		X				
S3			X		X		X	

i) Write down the forbidden latencies and initial collision vector.
ii) Draw the state diagram for scheduling the pipeline.
iii) Find out the simple cycle, greedy cycle and MAL.
iv) If the pipeline clock rate is 25 MHz, what is the throughput, efficiency and speed up of the pipeline?

8.a)	Explain memory hierarchy.	3	CO2
b)	What is set-associative mapping?	2	CO2
c)	A block-set associative cache memory consists of 128 blocks divided into four block sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words. i. How many bits are required for addressing the main memory? ii. How many bits are needed to represent the TAG, SET and WORD fields?	5	CO2
d)	Explain paging and segmentation.	5	CO2

9.a)	Describe Cache Coherency in Shared Memory architecture.	4	CO3
b)	Explain virtual memory.	3	CO3
c)	What is the significance of interconnection network in multiprocessor architecture?	3	CO3
d)	Explain any one static interconnection network	5	CO3
10.a)	What is the difference between CISC and RISC architecture?		
b)	What is the difference between array processor and vector processor?		
c)	Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order- 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7 If LRU replacement policy is used, which cache block will have memory block 7? Also, calculate the hit ratio and miss ratio.	4	CO2
11.	Write short note on**: (Any Three)**	3X5=15	
a)	Flynn's Taxonomy	5	CO4
b)	Memory Interleaving	5	CO3
c)	Linear vs. Non Linear pipeline	5	CO1
d)	Arithmetic pipeline	5	CO1
e)	Control Hazard	5	CO1