GURU NANAK INSTITUTE OF TECHNOLOGY An Autonomous Institute under MAKAUT 2022 **COMPUTER ARCHITECTURE**

CS401

TIME ALLOTTED: 3 Hours

FULL MARKS: 70

The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable

GROUP - A

(Multiple Choice Type Questions)

Answer any ten from the following, choosing the correct alternative of each question:

 $10 \times 1 = 10$

	7 1113 W	swer any ten from the following, endosing the correct alternative of each question		311.	
				Marks	CO No.
1.	(i)	Am	nultiprocessor system with common shared memory is called:	1	CO ₃
		a)	Loosely coupled system		
		b)	Tightly coupled system		
		c)	Both a and b		
		d)	None of the above		
	(ii)	Dire	ect mapping technique suffers from	1	CO ₃
		a)	Compulsory Miss		
		b)	Conflict Miss		
		c)	Coherence Miss		
		d)	All of the above		
	(iii)	Too	1	CO ₂	
		requ			
		a)	8		
		b)	16		
		c)	32		
		d)	64		
	(iv)	Asse	ociative memory is a	1	CO ₂
		a)	Pointer addressable memory		
		b)	Content addressable memory		
		c)	Very cheap memory		
		d)	Slow memory		
	(V)	The	largest delay in accessing data on a disk is due to	1	CO ₂
		a)	Seek time		
		b)	Rotation time		
		c)	data transfer time		
		d)	none of these		

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(vi)	Pipelining means		
	a) using more hardware for executing the desired task		
	b) an implementation technique in which multiple instructions are overlapped in execution.		
	c) the simultaneous execution of the same task (split up and	1	COI
	specially adapted) on multiple processors in order to obtain results		
	faster.		
	d) All of the above		
(vii)	Static pipelines are preferred when	1	CO ₁
	a) several functional configurations exist simultaneously		
	b) instructions of same type are to be executed continuously		
	c) Both are true		
	d) none is true		
(viii)		1	CO1
	a) Latency		
	b) Throughput		
	c) Latch Latency		
	d) None of the above		
(ix)	If the Main Memory, Cache memory size and block size are	1	CO ₂
	128KB, 16KB and 256B respectively, then the no. of Tag bits in		
	PA if Direct mapping technique is used-		
	a) 8		
	b) 6		
	c) 3		
	d) 17		2012-1
(x)	The performance of cache memory is frequently measured in terms of	1	CO2
	a) Locality of reference		
	b) Hit ratio		
	c) Mapping technique		
	d) Size of cache		
(xi)	represents an organization that includes many	1	CO ₂
	processing units under the supervision of a common control unit.		
	a) SISD		
	b) SIMD		
	c) MIMD		
	d) None of the above		
(xii)	What will be the speed up for a four-stage linear pipeline when the	1	CO ₂
	number of instruction n=64?		
	a) 4.5		
	b) 7.1		
	c) 6.5		
	d) 3.82		

GROUP – B (Short Answer Type Questions)

						Answer y three o				3 x 5	= 15
						,		01101111	67		
2	a)	What is h	nazard?							Marks	CO No.
-	b)							1 4	CO1		
	,=/	briefly.		ing tee	miqu	03 101 0	acii Oi	the ma	izaru type	4	COI
3	a)	What do				hput and	d Effi	ciency	?	4	CO1
	b)								1	CO1	
4	a)								2	COI	
	b)										CO1
5	a)	What are	the diffe	erent le	vels o	f paralle	elism')		2	CO4
	b)	Explain s	uper pip	elined	proces	ssor.				3	CO4
6		Consider	a fully a	ssociat	ive ca	che wit	h 8 ca	che blo	ocks (0-7). The	5	CO3
		memory block requests are in the order-									
		4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7 If LRU replacement policy is used, which cache block will have									
		memory b	placeme block 7?	Also, c	cy is i	ate the h	nich c	o and i	ock will have niss ratio.		
						GROU	JP - C	1 3			
						answer 7					
				(An	iswer a	any three	of the	e follow	ring)	$3 \times 15 = 45$	
7	a)	Evnlain T	hroughn	ut and	anaad		C	11	1 1 1	Marks	CO No.
6	u)	Explain Throughput and speedup ratio of pipelined architecture. i. Consider the following reservation table:							4	CO1	
			2	3	4	5	6	-			
		1	1					- 1	Q		
		1 S1 X	2	_		5		7	8 Y		
		S1 X			X	5	X	7	8 .X		
			X		X						
	b)	S1 X S2 S3	X	X		X	X	X	X	11	COI
	b)	S1 X S2 S3 i) Write exector.	X down the	X e forbic	lden l	X atencies	X and i	X nitial c	X ollision	11	CO1
	b)	S1 X S2 S3 i) Write ovector. ii) Draw	X down the	X e forbic te diagr	dden la	X atencies	X and i	X nitial c	X collision eline.	11	CO1
	b)	S1 X S2 S3 i) Write (vector. ii) Drav iii) Fin	X down the v the state d out the	X e forbic te diagr	lden la ram fo	X atencies or sched	X and i uling y cyc	X nitial c the pip le and	X collision eline.	11	CO1
	b)	S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If th	X down the state dout the pipeline	X e forbic te diagr e simple ne cloc	dden la ram fo e cycl k rate	X atencies or sched- e, greed is 25 M	and in uling by cyc	X nitial c the pip le and what is	X ollision eline. MAL. the	11	CO1
Q		S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If the	X down the state dout the pipelint, efficie	X e forbic te diagr e simple ne cloc	dden la ram fo e cycl k rate d spee	X atencies or sched- e, greed is 25 M ed up of	and in uling y cyc IHz, when p	X nitial c the pip le and what is	X ollision eline. MAL. the		
8	b) a)	S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If the throughput Explain pr	X down the state of the pipeling to efficie to operties	X e forbic te diagre e simple ne cloc ency and of mer	ram for e cyclok rated speed	X atencies or schedule, greed is 25 Med up of hierarch	and inguling by cyc IHz, withe py.	X nitial c the pip le and vhat is ipeline	X collision eline. MAL. the	11	CO1
8		S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If the throughput Explain proceeding	X down the state of out the pipelist, efficie roperties at the fo	X e forbic te diagre e simple ne cloc ency and of mer followir	ram for e cycle k rate d speed mory l	X atencies or schedule, greedule is 25 Mediup of hierarch primation	and inguling y cycles (Hz, volume) the p	X nitial c the pip le and vhat is ipeline	X collision eline. MAL. the ?		
8		S1 X S2 S3 i) Write ovector. ii) Draw iii) Fin iv) If the throughput Explain proceeding the address	X down the value of the state dout the pipeling t, efficience to the first for Dir	X te forbio te diagr e simple ne cloc ency and of mer followir rect maj	ram for e cyclic k rate d speed mory ling inforping.	X atencies or sched- e, greed is 25 M ed up of hierarch ormation , Associ	and inguling y cycles (Hz, volume) the p	X nitial c the pip le and vhat is ipeline	X collision eline. MAL. the		
8	a)	S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If the throughput Explain properties According the address Associative S2 S3 i) Write ovector.	X down the v the stat d out the ne pipelin t, efficie roperties g to the fo s for Dir re mappi	X te forbio te diagre e simple ne cloc ency and of mer followir rect may	ram for e cyclic k rate d speed mory ling information in the cyclic pping the sch	X atencies or schedule, greed is 25 Med up of hierarch ormation, Associemes:	and in uling y cyc IHz, which the property is a strice of the property of the	X nitial of the pip le and what is ipeline ermine mappin	ollision eline. MAL. the ? size fields in ng and Set-	3	CO2
8		S1 X S2 S3 i) Write ovector. ii) Drav iii) Fin iv) If the throughput Explain properties According the address Associative We	X down the v the stat d out the ne pipelin t, efficie roperties g to the fo s for Dir re mappi	X te forbic te diagre e simple ne cloc ency and of mer followir rect maj ng cach 6 MB n	ram for e cycle k rate d speed mory ling information pringen schmain main main main main main main main	X atencies or schedule, greed is 25 M and a portion of thierarch primation, Associatemes:	and in uling y cyc the p y. n, deterative and 1	X nitial countries of the pipule and what is ipeline ermine mappin MB C	X collision eline. MAL. the ?		
8	a)	S1 X S2 S3 i) Write ovector. ii) Draw iii) Fin iv) If the throughput Explain proceeding the address Associative — We — The	down the state of the pipeling to the for Direct mapping thave 250	X e forbic te diagre e simple ne cloc ency and of mer followir rect maj ng cacl 6 MB n space o	ram for e cyclic k rate d speed mory ling information main more pro-	X atencies or schedule, greedule is 25 Medup of hierarch ormation, Associemes: memory cessor is	and in uling y cyc the p y. n, deterative and 1	X nitial countries of the pipule and what is ipeline ermine mappin MB C	ollision eline. MAL. the ? size fields in ng and Set-	3	CO2
8	a)	S1 X S2 S3 i) Write (vector. ii) Drav iii) Fin iv) If the throughput Explain pr According the address Associative We The	down the state of the pipeling to the for Direct mapping address	X e forbio te diagree simple ne cloc ency and of mer followir rect may ng cacl 6 MB n space of ze is 12	ram for e cycle k rate d speed mory ling information in the schmain in the schmai	x atencies or schedule, greedule is 25 Med up of hierarch ormation, Associemes: memory cessor is es	and in uling y cyc IHz, which the property is and 1 s 256	X nitial countries of the pipule and what is ipeline ermine mappin MB C	ollision eline. MAL. the ? size fields in ng and Set-	3	CO2

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9	a)	Describe Cache Coherency in Shared Memory architecture.	5	CO4
	b)	Differentiate between NUMA and COMA Architecture.	5	CO4
	c)	Explain any one static interconnection network	5	CO4
10	a)	Differentiate between multiprocessor and multicomputer.	5	CO ₂
	b)	What is the difference between array processor and vector processor?	4	CO2
	c)	Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6 calculate the number of page faults using LRU and Optimal replacement policy.	6	CO2
11		Write short note on: (Any Three)	3x5=15	
	a)	Flynn's Taxonomy	5	CO4
	b)	Virtual Memory	5	CO3
	c)	VLIW processor	5	CO3
	d)	Pipelined floating-point adder	5	CO1
	e)	Omega network	5	CO5