GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2022
COMPUTER ARCHITECTURE
CS401

TIME ALLOTTED: 3 Hours **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

			Marks	CO No.
1.	(i)	A multiprocessor system with common shared memory is called: a) Loosely coupled system b) Tightly coupled system c) Both a and b d) None of the above	1	CO3
	(ii)	Direct mapping technique suffers from a) Compulsory Miss b) Conflict Miss c) Coherence Miss d) All of the above	1	CO3
	(iii)	To design a RAM of Size 1024X16 how many RAM chips are required of size 128X8? a) 8 b) 16 c) 32 d) 64	1	CO2
	(iv)	Associative memory is a a) Pointer addressable memory b) Content addressable memory c) Very cheap memory d) Slow memory	1	CO2
	(v)	The largest delay in accessing data on a disk is due to a) Seek time b) Rotation time c) data transfer time d) none of these	1	CO2

(vi)	Pipelining means a) using more hardware for executing the desired task b) an implementation technique in which multiple instructions are overlapped in execution. c) the simultaneous execution of the same task (split up and specially adapted) on multiple processors in order to obtain results faster. d) All of the above	1	CO1
(vii)	Static pipelines are preferred when a) several functional configurations exist simultaneously b) instructions of same type are to be executed continuously c) Both are true d) none is true	1	CO1
(viii)	..... is the rate at which operations get executed? a) Latency b) Throughput c) Latch Latency d) None of the above	1	CO1
(ix)	If the Main Memory, Cache memory size and block size are 128KB, 16KB and 256B respectively, then the no. of Tag bits in PA if Direct mapping technique is used- a) 8 b) 6 c) 3 d) 17	1	CO2
(x)	The performance of cache memory is frequently measured in terms of a) Locality of reference b) Hit ratio c) Mapping technique d) Size of cache	1	CO2
(xi)	.....represents an organization that includes many processing units under the supervision of a common control unit. a) SISD b) SIMD c) MIMD d) None of the above	1	CO2
(xii)	What will be the speed up for a four-stage linear pipeline when the number of instruction n=64? a) 4.5 b) 7.1 c) 6.5 d) 3.82	1	CO2

GROUP – B
(Short Answer Type Questions)
(Answer any *three* of the following) 3 x 5 = 15

			Marks	CO No.
2	a)	What is hazard?	1	CO1
	b)	Discuss the handling techniques for each of the hazard type briefly.	4	CO1
3	a)	What do you mean by Throughput and Efficiency?	4	CO1
	b)	What is prefetch buffer?	1	CO1
4	a)	State Amdahl's Law for maximum theoretical speedup.	2	CO1
	b)	Let a program have 40 percent of its code enhanced (f_E) to run 2.3 times faster (f_I). What is the overall system speedup S?	3	CO1
5	a)	What are the different levels of parallelism?	2	CO4
	b)	Explain super pipelined processor.	3	CO4
6		Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order- 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7 If LRU replacement policy is used, which cache block will have memory block 7? Also, calculate the hit ratio and miss ratio.	5	CO3

GROUP – C
(Long Answer Type Questions)
(Answer any *three* of the following) 3 x 15 = 45

			Marks	CO No.
7	a)	Explain Throughput and speedup ratio of pipelined architecture.	4	CO1
	b)	i. Consider the following reservation table:	11	CO1

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

i) Write down the forbidden latencies and initial collision vector.
ii) Draw the state diagram for scheduling the pipeline.
iii) Find out the simple cycle, greedy cycle and MAL.
iv) If the pipeline clock rate is 25 MHz, what is the throughput, efficiency and speed up of the pipeline?

8	a)	Explain properties of memory hierarchy.	3	CO2
	b)	According to the following information, determine size fields in the address for Direct mapping, Associative mapping and Set-Associative mapping cache schemes: – We have 256 MB main memory and 1 MB Cache memory – The address space of processor is 256 MB – The block size is 128 bytes – There are 8 blocks in a cache set.	9	CO2
	c)	Explain paging and segmentation.	3	CO2

9	a)	Describe Cache Coherency in Shared Memory architecture.	5	CO4
	b)	Differentiate between NUMA and COMA Architecture.	5	CO4
	c)	Explain any one static interconnection network	5	CO4
10	a)	Differentiate between multiprocessor and multicomputer.	5	CO2
	b)	What is the difference between array processor and vector processor?	4	CO2
	c)	Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6 calculate the number of page faults using LRU and Optimal replacement policy.	6	CO2
11		Write short note on: **(Any Three)**	3x5=15	
	a)	Flynn's Taxonomy	5	CO4
	b)	Virtual Memory	5	CO3
	c)	VLIW processor	5	CO3
	d)	Pipelined floating-point adder	5	CO1
	e)	Omega network	5	CO5