GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2021
COMPUTER ORGANIZATION & ARCHITECTURE
IT401

TIME ALLOTTED: 3HR **FULL MARKS:70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

			Marks	CO No
1.	(i)	The addressing mode, where you directly specify the operand value is----- a. Direct b. Immediate c. Relative d. Definite	1	CO3
	(ii)	Most of the time, computer instructions are divided into a. Function code b. Instruction code c. Operand d. Both function code and operand	1	CO4
	(iii)	The pseudo instruction used to load an address into the register is___ a. ADR b. LOAD c. ASSIGN d. PSLOAD	1	CO3
	(iv)	The offset used in the conditional branching is___ bit a. 24 b. 16 c. 24 d. 8	1	CO2
	(v)	What is the formula for Hit Ratio? a. Hit/(Hit + Miss) b. Miss/(Hit + Miss) c. (Hit + Miss)/Miss d. (Hit + Miss)/Hit	1	CO4
	(vi)	The main virtue for using single Bus structure is _____ a. Fast data transfers b. Cost effective connectivity and speed c. Cost effective connectivity and ease of attaching peripheral devices d. None of the mentioned	1	CO3

	(vii)	Which of the following Special purpose register holds the address of next instructions to be executed? a. Program Counter b. Instruction Register c. Stack pointer d. Base Register	1	CO2
	(viii)	A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor? a. Pointers b. Arrays c. Records d. All of these	1	CO4
	(ix)	Binary code which gives an actual instruction is called a. Function code b. Instruction code c. Logical code d. Address	1	CO2
	(x)	In which of these modes, the immediate operand is included in the instruction itself? a. Register operand mode b. Register and immediate operand mode c. Immediate operand mode d. None of the mentioned	1	CO4
	(xi)	What is the 2's complement representation of 24 in a 16 bit microprocessor a. 0000 0000 0001 1000 b. 1111 1111 1110 1000 c. 1111 1111 1110 0111 d. 0001 0001 1111 0011	1	CO1
	(xii)	The basic principle of Von-Neumann computer is a. Storing program and data in separate memory b. Using pipeline concept c. Storing program and data in same memory d. Using a large number of registers	1	CO3

GROUP – B

(Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

			Marks	**CO No**
2.	(a)	Explain the differences between RISC and CISC architecture.	2	CO2
	(b)	Draw the schematic diagram for daisy chain polling arrangement in case of vectored interrupt for three devices.	3	CO4
3.	(a)	Explain the role of operating system in computer system.	2	CO3
	(b)	Multiply (+15) and (-11) using Booth's algorithm.	3	CO5

4.	(a)	Explain Flynn's classification for multi process system.	3	CO4
	(b)	What do you mean by DMA?	2	CO3
5.	(a)	What is cache memory? What are the different mechanisms of writing into it?	3	CO4
	(b)	What is bus arbitration? Explain clearly.	2	CO3
6.	(a)	Explain the difference between three addresses, two addresses, one address, zero address instruction using suitable example.	2	CO4
	(b)	What do you mean by instruction cycle, machine cycle, T-state?	3	CO4

GROUP – C

(Long Answer Type Questions)

Answer any ***three*** from the following: **3×15=45**

			Marks	**CO No.**
7.	(a)	Differentiate between polled I/O and interrupt driven I/O.	6	CO4
	(b)	Write down the Booth's algorithm for multiplication of signed 2's complement numbers.	4	CO5
	(c)	Write down the flowchart of for division of two binary numbers using restoring division algorithm and explain it.	5	CO5
8.	(a)	Why does DRAM cell need refreshment?	4	CO4
	(b)	Describe the function of major components of digital computer with a block diagram.	6	CO1
	(c)	Differentiate between SRAM and DRAM.	5	CO1
9.	(a)	Explain the difference between instruction pipeline and arithmetic pipeline.	4	CO5
	(b)	What are advantages of relative addressing mode over direct addressing mode?	5	CO3
	(c)	Differentiate Centralized shared- memory architecture, Distributed shared-memory architecture.	6	CO2
10.	(a)	With the help of neat diagram show the structure of a typical arithmetic pipeline performing A*B+C.	4	CO5
	(b)	What is the bandwidth of a memory system that transfers 128 bits data per reference having a speed of 20 nano sec per operation?	4	CO3
	(c)	What do you mean by physical address space and logical address space? Explain with an example how logical address is converted into physical address and explain how page replacements take place.	7	CO4
11.		Write down the short notes on any three of the followings;	3*5=15	
	(a)	Set Associative mapping	5	CO4
	(b)	Addressing Modes	5	CO3
	(c)	EEPROM	5	CO1
	(d)	Virtual Memory	5	CO1