GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2022
COMPUTER ORGANIZATION & ARCHITECTURE
IT401

TIME ALLOTTED: 3 HOURS **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ten from the following, choosing the correct alternative of each question: 10×1=10

			Marks	CO No
1.	(i)	Which Register is used to storing the address of the next instruction to be executed a. Program Counter b. Stack Pointer c. Address Register d. Instruction Registe	1	CO3
	(ii)	Most of the time, computer instructions are divided into a. Function code b. Instruction code c. Operand d. Both function code and operand	1	CO4
	(iii)	The pseudo instruction used to load an address into the Register is___ a. ADR b. LOAD c. ASSIGN d. UPLOAD	1	CO3
	(iv)	The offset used in the conditional branching is___ bit a. 24 b. 16 c. 24 d. 8	1	CO2
	(v)	What is the formula for Hit Ratio? a. Hit/(Hit + Miss) b. Miss/(Hit + Miss) c. (Hit + Miss)/Miss d. (Hit + Miss)/Hit	1	CO4
	(vi)	The main virtue for using single Bus structure is	1	CO3

a. Fast data transfers
b. Cost-effective connectivity and speed
c. Cost-effective connectivity and ease of attaching peripheral devices
d. None of the mentioned

(vii)	The user's view of memory is supported by a. Paging b. Segmentation c. Both d. None of these	1	CO2
(viii)	A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor? a. Pointers b. Arrays c. Records d. All of these	1	CO4
(ix)	Binary code which gives an actual instruction is called a. Function code b. Instruction code c. Logical code d. Address	1	CO2
(x)	In which of the following modes is the immediate operand included in the instruction? a. Register operand mode b. Register and immediate operand mode c. Immediate operand mode d. None of the mentioned	1	CO4
(xi)	What is the 2's complement representation of 24 in a 16-bit microprocessor a. 0000 0000 0001 1000 b. 1111 1111 1110 1000 c. 1111 1111 1110 0111 d. 0001 0001 1111 0011	1	CO1
(xii)	Associative memory is an a. Pointer addressable memory b. Very cheap memory c. Content addressable d. Slow memory	1	CO5

GROUP – B
(Short Answer Type Questions)
Answer any ***three*** from the following: **3×5=15**

			Marks	CO No
2.	(a)	Compare RISC and CISC.	2	CO3
	(b)	Two 1024X4 bits RAM chips are given. Design a memory of size 2048X8 bits.	3	CO4
3	(a)	Multiply (+15) and (-11) using Booth's algorithm.	5	CO5
4.	(a)	Explain Flynn's classification for the multi-process system.	3	CO4
	(b)	What do you mean by MDR?	2	CO3
5.	(a)	What is cache memory? Explain memory write operation.	3	CO4
	(b)	Explain memory read operation?	2	CO3
6.	(a)	Briefly explain the IEEE 754 standard format for floating-point number representation.	2	CO4
	(b)	Represent the decimal value (-7.5) in IEEE single-precision format.	3	CO4

GROUP – C
(Long Answer Type Questions)
Answer any ***three*** from the following: **3×15=45**

			Marks	CO No.
7.	(a)	Explain the advantages of Carry's look ahead adder over Carry Propagator adder.	6	CO4
	(b)	Explain "NINE" property of cache memory?	4	CO5
	(c)	A Computer has 512 KB cache memory and 2 MB main memory. If the block size is 64 bytes, then find out the subfield for a. Direct Mapped Cache b. Associative Cache c. 8-way set associative Cache	5	CO5
8.	(a)	Why does DRAM cell need refreshment?	4	CO4
	(b)	Explain immediate, direct, implied, register indirect and relative addressing modes with example	6	CO1
	(c)	Differentiate between SRAM and DRAM.	5	CO1
9.	(a)	Explain the difference between an instruction pipeline and an arithmetic pipeline.	4	CO5
	(b)	What are the advantages of relative addressing mode over direct addressing mode?	5	CO3
	(c)	Explain the basic DMA operations for data transfer between memory and peripherals.	6	CO4

10.	(a)	Consider page reference string 1, 3, 0, 3, 5, 6, 3 with 3 page frames. Find the number of page faults for LRU page replacement algorithm.,	5	CO5
	(b)	You are required to write a program segment that can perform the operation C ← A+B (a) A machine with one-address instructions (b) A machine with one-and-half instructions (c) A machine with two-address instructions (d) A machine with three-address instructions (e) A machine with zero-address instructions	10	CO3
11.		Write down the short notes on any three of the followings;	3x5=15	
	(a)	EEPROM	5	CO1
	(b)	Addressing Modes	5	CO3
	(c)	Set Associative mapping	5	CO4
	(d)	Bus organization using tri-state buffer	5	CO2
	(e)	VLIW Architecture	5	CO4