# GURU NANAK INSTITUTE OF TECHNOLOGY

## An Autonomous Institute under MAKAUT

## 2021

## DIGITAL ELECTRONICS

## EE403

**TIME ALLOTTED: 3HR** **FULL MARKS:70**

***The figures in the margin indicate full marks.***

***Candidates are required to give their answers in their own words as far as practicable***

**GROUP – A**

**(Multiple Choice Type Questions)**

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

| | | | Marks | CO No. |
|---|---|---|---|---|
| 1. | (i) | The SR latch consists of _____<br>a) 1 input<br>b) 3 inputs<br>c) 2 inputs<br>d) 4 inputs | 1 | CO4 |
| | (ii) | The SOP form of logical expression is most suitable for designing logic circuits using only<br>a) XOR gate<br>b) NOR gate<br>c) OR gate<br>d) AND gate | 1 | CO2 |
| | (iii) | The fastest logic gate family is<br>a) CMOS<br>b) ECL<br>c) TTL<br>d) RTL | 1 | CO4 |
| | (iv) | Race condition is avoided by<br>a) J-K flip flop<br>b) Master Slave flip flop<br>c) D flip flop<br>d) S-R flip flop | 1 | CO3 |
| | (v) | Gray code for $(1011)_2$ is<br>a) 1000<br>b) 1101<br>c) 1110<br>d) None of these | 1 | CO1 |
| | (vi) | The SOP form of logical expression is most suitable for designing logic circuits using only<br>a) XOR gates<br>b) AND gates<br>c) OR gates<br>d) NAND gates | 1 | CO2 |
| | (vii) | D-flip flop can be used as<br>a) Divider circuit<br>b) Delay switch<br>c) Differentiator<br>d) None of these | 1 | CO3 |

| | | | |
|---|---|---|---|
| (viii) | What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?<br>a) SIPO<br>b) PIPO<br>c) SISO<br>d) PISO | 1 | CO3 |
| (ix) | What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?<br>a) SIPO<br>b) PIPO<br>c) SISO<br>d) PISO | 1 | CO3 |
| (x) | In 4-to-1 multiplexer, if S1 = 1 & S0 = 1, then the output will be<br>a) Y0<br>b) Y1<br>c) Y2<br>d) Y3 | 1 | CO3 |
| (xi) | Excess code representation of decimal 984 is<br>a) 101110101101<br>b) 110010110111<br>c) 11010011010<br>d) 110111110111 | 1 | CO1 |
| (xii) | 2's complement of 1010111 is<br>a) 0101001<br>b) 0110110<br>c) 0101100<br>d) 0101101 | 1 | CO1 |

## GROUP – B
## (Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

| | | Marks | CO No. |
|---|---|---|---|
| 2. | Perform 2's complement subtraction of 010110-100101 | 5 | CO1 |
| 3. | Prove the following (A+B) ((AC)'+C) (B'+AC)'=A'B | 5 | CO2 |
| 4. | Write the logic gate diagram of 1*4 Demultiplexer. | 5 | CO3 |
| 5. | Perform the following operations:<br>(i) Convert Decimal 928 into Hexa decimal<br>(ii) Convert Hexa decimal 7AC .39 to the Binary<br>(iii) Subtract 1101 from 1111 using 2's complement | 5 | CO1,CO2 |
| 6. | Minimize the following boolean function- using Kmap<br>$F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 10, 13, 15)$ | 5 | CO1,CO2 |

## GROUP – C
## (Long Answer Type Questions)

Answer any ***three*** from the following: **3×15=45**

| | | | Marks | CO No. |
|---|---|---|---|---|
| 7. | (a) | Describe the bidirectional shift register with the help of circuit diagram. | 5 | CO3 |

(b) The figure below shows a full adder truth table — 10 — CO3

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | $C_{in}$ | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

(i) Write down the Boolean expressions for the sum bit and the carry output bit
(ii) Construct a full adder using combination of **AND, XOR** and **OR** gates.

8. (a) What is difference between combinational and sequential circuits? — 6 — CO3

(b) Simplify **f = A'BC' + AB'C +ABC** using: — 9 — CO1
(a) Sum of minterms. (b) Maxterms

9. (a) Why parity checking is required? — 2 — CO3

(b) Find the expression for segment "b", "d" and "g" of a BCD 7 segment display. — 8 — CO3

(c) Design a 4 bit up down counter. — 5 — CO3

10. (a) What do you mean by Race around condition of Flip-flop? — 3 — CO3

(b) Design a Master Slave Flip-flop and discuss its operation. — 5 — CO3

(c) Design a circuit to convert Binary to Grey code. — 7 — CO3

11. (a) Shift register — 5 — CO4

(b) PROM — 5 — CO4

(c) Demultiplexer — 5 — CO3

(d) D/A & A/D Converters — 5 — CO4

(e) TTL — 5 — CO4