GURU NANAK INSTITUTE OF TECHNOLOGY An Autonomous Institute under MAKAUT 2022

MICROPROCESSOR AND MICROCONTRILLER CS602

TIME ALLOTTED: 3 HOURS

FULL MARKS: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable

GROUP - A

(Multiple Choice Type Questions)

Answer any ten from the following, choosing the correct alternative of each question: 10×1=10

1. (i) A single instruction to clear the lower four bits of the accumulator in 8085 microprocessor is a) XRI OFH b) ANI OFH c) XRI FOH d) ANI FOH (ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair d) HL-pair & memory location	CO2
a) XRI OFH b) ANI OFH c) XRI FOH d) ANI FOH (ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair	
b) ANI OFH c) XRI FOH d) ANI FOH (ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair	
c) XRI FOH d) ANI FOH (ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair	
d) ANI FOH (ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair	
(ii) The instruction XCHG exchanged the contents of a) Accumulator & H b) DE-pair & HL pair c) BC-pair & HL pair	
a) Accumulator & Hb) DE-pair & HL pairc) BC-pair & HL pair	
b) DE-pair & HL pair c) BC-pair & HL pair	CO2
b) DE-pair & HL pair c) BC-pair & HL pair	
c) BC-pair & HL pair	
d) HL-pair & memory location	
(iii) The number of programmable 8-bit register of 8085 microprocessor is	COI
a) 5	
b) 6	
c) 7	
d) 8	
(iv) In order to enable TRAP interrupt, which of the following instructions is /are	CO1
needed?	
a) El only	
b) SIM only	
c) EI & SIM	
d) None of the mentioned	
(v) What is the vector call location of the non-maskable interrupt of 8085?	COI
a) 0000 _H	
b) 0024 _H	
c) 0020 _H	
d) 0034 _H	

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(vi)	Full fo	rm of PSW is		1	COL
	a)	Program Specific Word			
	b)	Program Status Word			
	c)	Processor Status Word			
	d)	Processor Specific Word			
(vii)	If curre	ent content of register D is 00 _H , then after execu	tion of the instruction DCR D	1	CO2
		ntent of D will be			
	a)	01 _H			
	b)	0F _H			
	c)	FO _H			
	d)	neither 01 _H nor 0F _H nor F0 _H			
(viii)	Which	one of the following is the non-vectored interru	pt of 8085 microprocessor?	1	COI
	a)	TRAP			
		EI			
	c)	INTR			
	d)	RIM			
(ix)	T-State	es in 'CALL' instruction of 8085 MPU are		1	CO ₃
	a)	13			
	b)	18			
	c)	10			
	d)	7			
			W.		
(x)	Addres	ss lines required for 32K byte memory chip are		1	COL
		13			
		14			
	c)	15			
	d)	16			
(xi)	What	will be content of Z flag and P flag if result	is all 0 after any arithmetic	1	CO ₂
	instruc				
		Z=0, P=0			
	b)	Z=0, P=1			
		Z=1, P=0			
	d)	Z=1, P=1			
(xii)	The S	egment and Offset address of the instruction	on to be executed by 8086	1	COI
		rocessor are pointed by			
		CS AND SI			
	b)	DS and IP			
	c)	CS and SP			
		CS and IP			

 $3 \times 15 = 45$

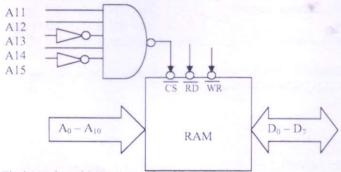
GROUP - B (Short Answer Type Questions) Answer any three from the following

 $3 \times 5 = 15$

			Marks	CO No.
2.	a.	Explain PSW.	1	CO2
	b.	Write an assembly language program to reset all bits of Flag Register of 8085	4	CO2
3.		Explain the structure of flag register of 8085 with proper diagram and example.	5	COI
4.	a.	What are RIM & SIM?	1	COI
	b.	Explain the function of RIM & SIM.	4	COI
5.	a.	What is the operating frequency of 8085 µp?	1	CO1
	b.	Write down the differences between hardware and software interrupt with example	4	CO3
6.		Write short notes on MIN/MAX operation of 8086 microprocessor.	5	COI
		GROUP - C		

(Long Answer Type Questions) Answer any three from the following

Marks CO No. What do you mean by instruction cycle, machine cycle and T-states? CO3 Draw the timing diagram of the following instruction: 8 CO₃ 8005: STA 9250 CO3 A11



Find out the address range for this RAM chip.

Memory Address in Hex	Mnemonics in HEX	
C000	LXI SP, FFFF	
C003	LXI B, 1234	
C006	MVI A, 05	
C008	CALL A010	
C00B	MOV B, C	
C00C	HLT	
A010	PUSH B	
A011	POP PSW	
A012	MVI C,56	
A014	RET	

Consider the above program and answer the following five question:

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	b.	What is the value of PC after completion of execution of CALL instruction? What will be content of SP after the execution of the program? What will be content of A-F pair after the execution of the program? Specify the stack locations where the contents of register pair B-C are stored. Assuming before CALL A010, the stack is not used, specify the contents of top two locations after completion of the execution of instruction POP PSW Describe the sequence of events done in the execution of the following instruction:		CO2 CO2 CO2 CO2 CO2
		9AFE: CALL 8B75		
9.	a.	Evolain I DAV VDA CMB instruction 12	3	-
	b.	Explain LDAX, XRA, CMP instruction with proper example	6	CO ₂
	U.	The length is given in the location 912F and the series itself starts from 9130. Store the result at 9200.	5	CO ₂
	C.	Calculate the time delay incurred in the following delay routine:	4	CO2
		LXI C, 34 LOOP: DCR C JNZ LOOP		
		Assume the microprocessor has an operating frequency 2 MHz.		
10.	a.	Describe the different addressing modes of 8086 up.	4	CO1
	b.	What are the main function performed by BIU and EU operational unit of 8086 µp?	8	COI
	C.	How pipelining achieved in 8086 microprocessor?	3	COI
11.		Short note (Answer any three)	3x5=15	
	a.			CO1
	b.	8086 Flag Register	5	CO1
	C.	Vectored vs Non-vectored Interrupts.	5	COI
	d.	Demultiplexing of the bus AD ₇ -AD ₀ in 8085 Microprocessor	5	CO1
	e.	Addressing modes of 8085	5	CO3