GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2022
VLSI & MICROELECTRONICS
EC601

TIME ALLOTTED: 3 HOURS **FULL MARKS: 70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)
Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

			Marks	CO No
1.	(i)	Dynamic power in CMOS gate is proportional to (a) VDD2 (b) VDD (c) VDD-1 (d) VDD1/2	1	CO1
	(ii)	In a DRAM cell information is stored across (a) Inductor (b) Capacitor (c) Resistor (d) Thermistor	1	CO2
	(iii)	Which one is correct? (a) NMOS can pass logic one without any degradation (b) Both NMOS and PMOS can pass logic one without any degradation (c) PMOS can pass logic one without any degradation (d) PMOS can pass logic zero without any degradation	1	CO1
	(iv)	_____ can pass a logic 1 perfectly, but cannot pass a logic 0 perfectly. (a) nMOS transistor (b) pMOS transistor (c) CMOS transistor (d) none of these	1	CO3
	(v)	The ON-resistance of a MOSFET _____ . (a) linearly increases with V_{gs} (b) linearly decreases with Vgs (c) exponentially increases with V_{gs} (d) non-linearly decreases with V_{gs}	1	CO3
	(vi)	Drift current dominates at (a) strong inversion (b) weak inversion (c) strong and weak inversion both (d) cannot be determined	1	CO3

(vii)	For a 0.5 μm process technology _____. (a) $\lambda = 0.25$ μm (b) $\lambda = 0.5$ μm (c) $\lambda = 1$ μm (d) $\lambda = 0.125$ μm		1	CO4
(viii)	In MOSFET fabrication, the channel length is defined during the process of (a) Isolation oxide growth (b)Channel stop implantation (c) Poly – silicon gate patterning (d)Lithography step leading to the contact pads		1	CO3
(ix)	Unit of sheet resistance is _____ . (a) ohm/square (b) ohm (c) ohm m (d) ohm/m		1	CO4
(x)	In constant voltage scaling, the doping density (a) remains unchanged (b) increases by a factor s (c) increases by a factor s^2 (d) increases by a factor s^3		1	CO1
(xi)	Critical path delay is the _____ . (a) longest path delay (b) smallest path delay (c) optimum path delay (d) none of these		1	CO5
(xii)	Slack is defined as the time difference between (a) the earliest required time and the latest arrival time at any node (b) the latest required time and the earliest arrival time at any node (c) the latest required time and the latest arrival time at any node (d) the earliest required		1	CO5

GROUP – B
(Short Answer Type Questions)
Answer any ***three*** from the following: **3×5=15**

			Marks	CO No
2.		Implement the 2:1 MUX using Transmission Gate.	5	CO2
3.	(a)	What do you mean by MOSFET scaling?	1	CO1
	(b)	What are the different types of scaling techniques	4	CO1
4.		Design of CMOS S-R & J-K Latch (Clocked & without Clock)	5	CO2
5.		Draw the complete small signal model of MOSFET and describe.	5	CO3
6.		Discuss the layout design rules.	5	CO4

GROUP – C
(Long Answer Type Questions)
Answer any ***three*** from the following: **3×15=45**

			Marks	CO No
7.	(a)	Draw the Y-chart and explain the VLSI design process.	7	CO1
	(b)	What do you mean by drain-induced barrier lowering (DIBL)?	4	CO1
	(c)	Describe static and dynamic power dissipation in CMOS.	4	CO5
8.	(a)	Define the terms: Critical path, arrival time, slack, skew, set-up time, hold time.	5	CO5
	(b)	Design a CPL NAND GATE and CPL NOR GATE.	5	CO2
	(c)	Explain the critical voltages and Noise Margin using VTC of CMOS inverter.	5	CO2
9.	(a)	Draw the stick diagram of Z= [A(D+E)+BC]'	5	CO4
	(b)	Draw the circuit, stick diagram and layout of CMOS NAND gate and NOR GATE	10	CO4
10.	(a)	Explain the operation of the MOS voltage reference circuit with circuit diagram	7	CO3
	(b)	Draw a CMOS differential amplifier and explain its operation.	8	CO3
11.		Write short notes on any three	3x5=15	
	(a)	CMOS-n well & p well fabrication process	5	CO4
	(b)	Current sources and current sink	5	CO3
	(c)	FPGA architecture	5	CO1
	(d)	NORA logic	5	CO2