GURU NANAK INSTITUTE OF TECHNOLOGY
An Autonomous Institute under MAKAUT
2021
VLSI & MICROELECTRONICS
EC(EI)802B

TIME ALLOTTED:3HR **FULL MARKS:70**

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP – A
(Multiple Choice Type Questions)

Answer any ***ten*** from the following, choosing the correct alternative of each question: **10×1=10**

		Marks	CO No
1. i)	MOS transistor a. Has only one p-n junction. b. Has only two electrodes. c. Gate electrode is in direct contact with silicon. d. Conducts when sufficient voltage is applied to gate electrode.	1	CO1
(ii)	When Pull Down and Pull Up are parallel, they form a. OR gate b. NOT gate c. AND gate d. NAND gate	1	CO6
(iii)	MOSFETs can be operated at higher frequencies as compared to BJTs because a. MOSFETs have higher input impedance b. MOSFETs are voltage controlled c. MOSFETs have positive temperature coefficients d. Minority carriers storage time is absent in MOSFETS.	1	CO1
(iv)	Which occupies lesser area? a. nMOS b. pMOS c. CMOS d. BiCMOS	1	CO3
(v)	Outputs of the AND gate in PLD is known as _____ a. Input lines b. Output lines c. Strobe lines d. Control lines	1	CO1
(vi)	Noise Margin is : a. Amount of noise the logic circuit can withstand b. Difference between VOH and VIH c. Difference between VIL and VOL d. All of the Mentioned	1	CO2

(vii)	PLA is used to implement _____ a. A complex sequential circuit b. A simple sequential circuit c. A complex combinational circuit d. A simple combinational circuit	1	CO6
(viii)	Which among the following is/are regarded as an/the active resistor/s? a. MOS diode b. MOS transistor c. MOS switch d. All of the above	1	CO1
(ix)	CMOS domino logic is same as _____ with inverter at the output line a. clocked CMOS logic b. dynamic CMOS logic c. gate logic d. switch logic	1	CO3
(x)	In two-stage op-amp, what is the purpose of compensation circuitry? a. To provide high gain b. To lower output resistance & maintain large signal swing c. To establish proper operating point for each transistor in its quiescent state d. To achieve stable closed-loop performance	1	CO5
(xi)	In CMOS static logic design, total number of transistors required for the Boolean function F = A + (B + CD) is a. 10 b. 8 c. 5 d. None of these	1	CO5
(xii)	Switching speed of a MOS device depends on a. gate voltage above threshold b. carrier mobility c. length channel d. All of the mentioned	1	CO1

GROUP – B
(Short Answer Type Questions)

Answer any ***three*** from the following: **3×5=15**

		Marks	CO No
2.	How do you expect the gate source capacitance of a MOSFET to vary with gate source voltage? Explain your answer.	5	CO2
3.	Draw the Y-chart and explain the VLSI design process.	5	CO6
4.	With a suitable diagram briefly describe the p-well fabrication process of a CMOS inverter.	5	CO2

5.	Draw the layout & Schematic diagram of a static CMOS NAND/NOR gate & identify the corresponding components in the two drawing.	5	CO3
6.	Which current is dominant in MOSFET? Drift or diffusion?	5	CO4

GROUP – C
(Long Answer Type Questions)

(Answer any *three* of the following) **3 x 15 = 45**

		Marks	CO No
7. a)	Draw the stick diagram of Z= [A(D+E)+BC]	9	CO1
b)	Implement a D- Flip Flop using transmission gate	6	CO1
8. a)	Design a CMOS FULL-ADDER circuit.	10	CO2
b)	Draw the layout of CMOS NAND gate.	5	
9. a)	Define a current sink/source. Obtain the expressions for small signal output resistance of an n-channel MOSFET. Show how the output resistance of a current sink can be increased. Explain how a current mirror can be used as a current amplifier.	8	CO4
b)	Explain with a circuit diagram the operation of a differential amplifier and draw its voltage characteristics. What does CMMR mean for a differential amplifier?	7	CO4
10. a)	Explain the process, temperature, and voltage dependency of propagation delay.	5	CO6
b)	Derive the expression for logical effort. Explain why NAND is preferred over NOR gate using the concept of logical effort.	5	CO6
c)	Derive the expressions for rise and fall time of an inverter circuit.	5	CO6
11.	Short notes on: (Answer any three)	3X5=15	
a)	Photolithography	5	CO4
b)	Silicon on insulator	5	CO2
c)	Series-Parallel switched capacitor circuit	5	CO4
d)	Twin Tub Fabrication Process	5	CO2
e)	FPGA architecture	5	CO2